

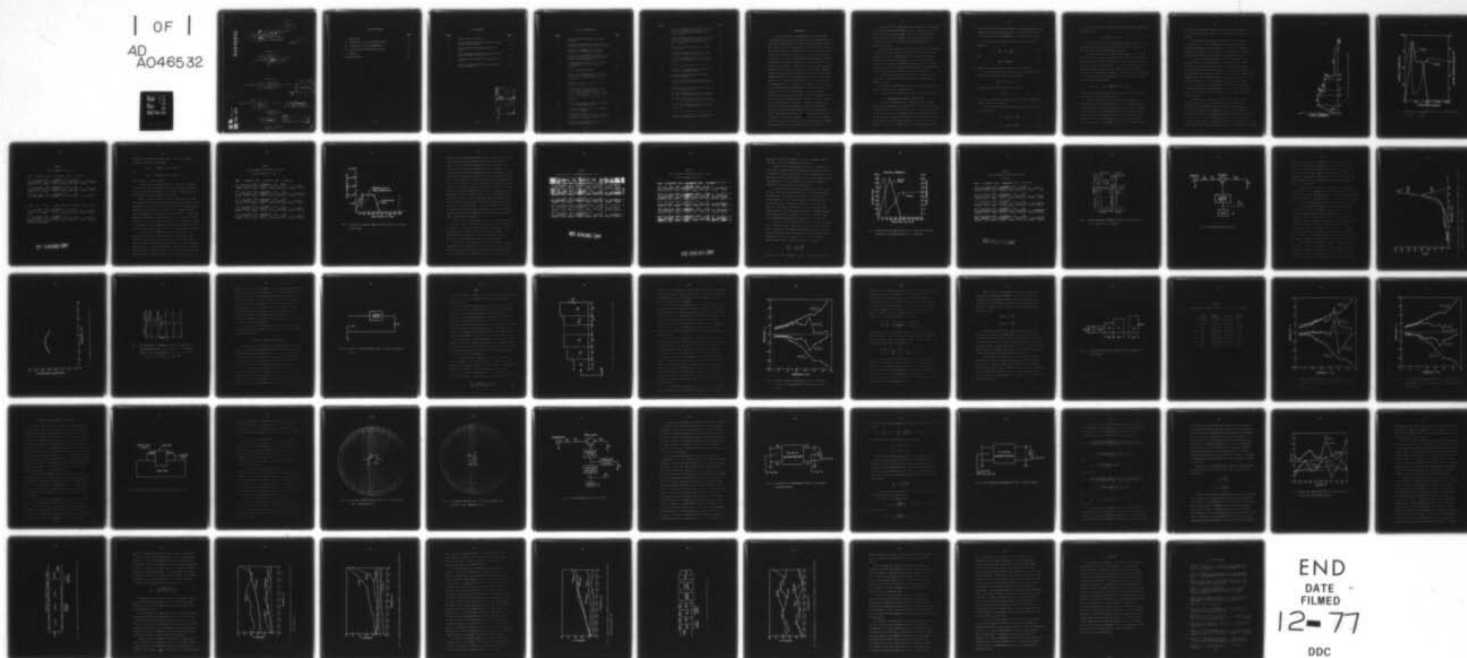
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TRAPATT DIODE AMPLIFIERS.(U)
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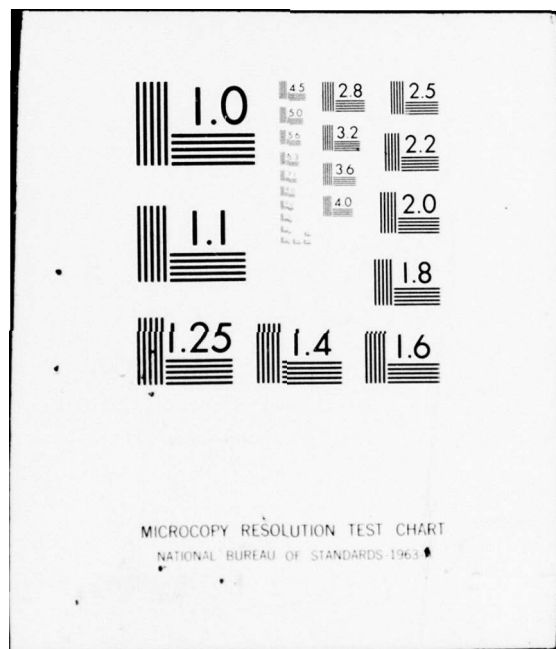
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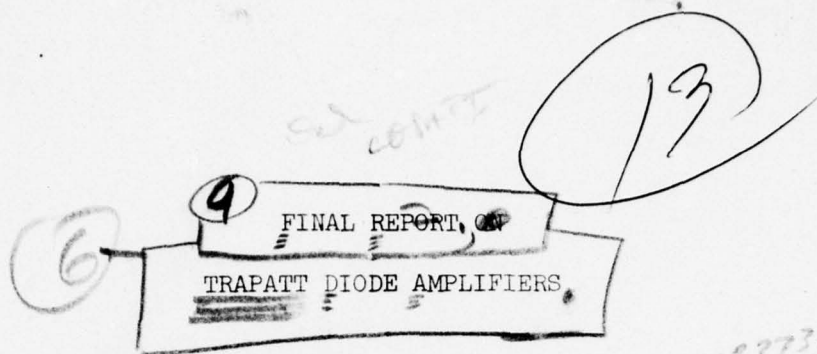


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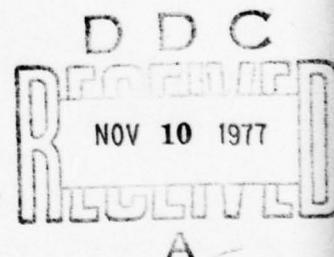
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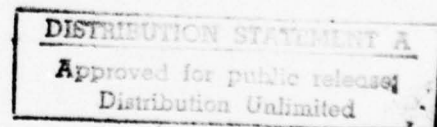
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I. INTRODUCTION

Since the discovery of the TRAPATT mode of operation many investigators have attempted to develop broad-band TRAPATT amplifiers. Gibbons and Grace¹ constructed an X-band amplifier having a saturated power output of 19 W, 7 dB gain and 29 percent efficiency at 8.6 GHz. The device was tested in an X-band reflection type amplifier circuit operating at a duty factor of less than 1 percent and a bias pulse width of 0.2 μ s. Cox et al.² developed a TRAPATT amplifier operating between 8 and 8.5 GHz with peak power output as high as 34 W and 12 to 16 percent efficiency. Fong and Ying³ used both n-type and p-type TRAPATT diodes in a coaxial air-line circuit employing an impedance transformer close to the diode and two tuning slugs. For the n-type TRAPATT operating at 5 GHz the peak power was typically 18 to 25 W, the gain 5 to 7 dB, the dc-RF efficiency 25 to 30 percent and the 3-dB bandwidth was 3 to 5 percent. The comparable results for the p-type TRAPATT amplifier operating at 8.73 GHz was 2 to 4 W, 4 to 9 dB gain, 18.5 percent efficiency and 2 to 7 percent bandwidth. Additional work by Fong et al.⁴ using a fix-tuned MIC amplifier circuit resulted in approximately 90 W, 5 dB gain, 20 percent efficiency and a 3-dB bandwidth of 17 percent. It should be emphasized that these results were obtained without the benefit of any tuning. However, considerable work was devoted to characterizing the circuit using a network analyzer, and to circuit modeling with the aid of a computer. It was evident from these results, as well as from the work of others, that the circuit is the dominating factor in TRAPATT operation whether it be as an oscillator or as an amplifier.

Curtice et al.⁵ utilized the second-harmonic-extraction approach to develop an X-band TRAPATT amplifier. They designed the device such that the RF input and output signals were twice the TRAPATT fundamental frequency. Typical results for their amplifier were 10 to 12 W, 6 dB gain, 10 percent efficiency and a 200 MHz bandwidth at approximately 8 GHz.

There have been numerous other recent investigations on TRAPATT amplifiers but in every case one of the major obstacles has been the inability to create a broad-band amplifier. Progress has been made but the problems are far from being resolved. The purpose of this program was to determine theoretically and experimentally the circuit characteristics needed to achieve broadband amplification with TRAPATT diodes. The investigation was divided into three main steps:

1. Theoretical determination using computer simulation of the required real and imaginary parts as a function of frequency for the amplifier circuit.
2. Synthesis of amplifier circuits, if realizable, which would match the required circuit characteristics.
3. Construction and testing of the circuit designs obtained in 2.

II. DETERMINATION OF CIRCUIT CHARACTERISTICS

To model the TRAPATT device, a computer simulation program developed by Paul Bauhahn of the Electron Physics Laboratory was used.⁶ The numerical method is explicit in the drift current and half implicit in the diffusion current. The method begins by assuming that n and p (electron and hole densities), J_N and J_P (electron and hole currents) and E (electric field) are known throughout the diode at one particular time. Also, the terminal voltage, V_T , which exists across the

diode at the next time step is specified. Given this information, the simulation calculates the diode current at the next time step. The actual sequence of steps implemented by the program is as follows:

1. p and n are calculated at the next time step using the equations

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \frac{\partial JP}{\partial x} + G \quad (1)$$

and

$$\frac{\partial n}{\partial t} = \frac{1}{q} \frac{\partial JN}{\partial x} + G, \quad (2)$$

where G is the generation due to avalanche multiplication.

2. The electric field E is calculated at the next time step from Poisson's equation (once n and p are determined)

$$\frac{\partial E}{\partial x} = \frac{q}{\epsilon} (p - n + N - P) \quad (3)$$

The electric field must also satisfy the equation

$$\int_0^W E \, dx = V_T, \quad (4)$$

where N and P represent the doping densities N_d and N_A , respectively, and W the length of the diode.

3. The currents JN and JP at the next time step are calculated from the equations

$$JN = q\mu_n nE + qD_n \frac{\partial n}{\partial x} \quad (5)$$

and

$$JP = q\mu_p pE - qD_p \frac{\partial p}{\partial x} \quad (6)$$

4. The terminal current (not including the displacement component) is calculated from

$$J_T = \frac{1}{W} \int_0^W (J_N + J_P) dx \quad (7)$$

At this point the cycle is repeated, the terminal voltage for the next time step (two steps ahead of the starting time) is specified, and the current for this time step is again calculated.

The above simulation is a voltage-driven scheme; i.e., the diode terminal voltage is specified as a function of time and the resulting diode current is calculated as a function of time. However, the program can also be used with a current drive. In this case JDRIVE(t) is the driving current at a particular time t, while JT(t) is the terminal current less the displacement component as calculated in 4. The difference in these quantities yields the displacement current so that the voltage V_T at the next time step becomes

$$V_T(t + \Delta t) \approx V_T(t) + \frac{\Delta t}{C_d} [JDRIVE(t) - JT(t)] \quad (8)$$

where C_d is the diode capacitance ϵ/W plus any additional capacitance which might be in parallel with the diode.

Whether a current drive or a voltage drive is used for the TRAPATT cycle, two major problems arise, that of convergence and that of realizability. For example, if a periodic current drive is applied to the device, the resulting voltage waveform should also be periodic. In fact the state of the diode at time t should be identical in all respects to the state of the diode at times $t + nT$, where T is the current period and n is any integer. The problem of convergence is a

difficult one for TRAPATT operation because avalanche multiplication is a random process which tends to work against any periodicity of the solution.

Even after convergence has been obtained, the solution may not be realizable, i.e., a Fourier analysis of the resulting voltage and current waveforms may not yield a negative resistance at all harmonic frequencies considered. This is the case for the idealized step current waveforms that have been used in some previous TRAPATT analyses.^{7,8}

A number of different techniques have been formulated to bring about convergence in the TRAPATT cycle. These techniques use either a current-driven or a voltage-driven scheme. The general current drive waveform used in the simulations described in this report is shown in Fig. 1. The amplitudes of the various sections, A_1 , A_2 and A_3 , and the angles of the segments connecting the constant amplitude sections, θ_1 , θ_2 and θ_3 , are all variable parameters. Once these parameters have been set, the times $t_1 - t_5$ are determined during a preliminary simulation to guarantee that the voltage recovers at t_5 approximately to its initial value at $t = 0$. A_3 is low (~ 100 A/cm²) so that the voltage does not change significantly between t_5 and T .

An example of a converged solution using this type of current drive is shown in Fig. 2. The voltage and current waveforms were Fourier analyzed to obtain the diode impedance and power generated at the first five harmonics; the results are given in Table 1, where F is frequency in GHz, PRF is power generated in W/cm², EFF is the efficiency in percent, G and B are the real and imaginary parts of the admittance in mhos/cm², and R and X are the corresponding impedance components in Ω /cm². $VTAMP$, $VTANG$, $JIAMP$ and $JIANG$ describe the amplitudes and phases of the Fourier

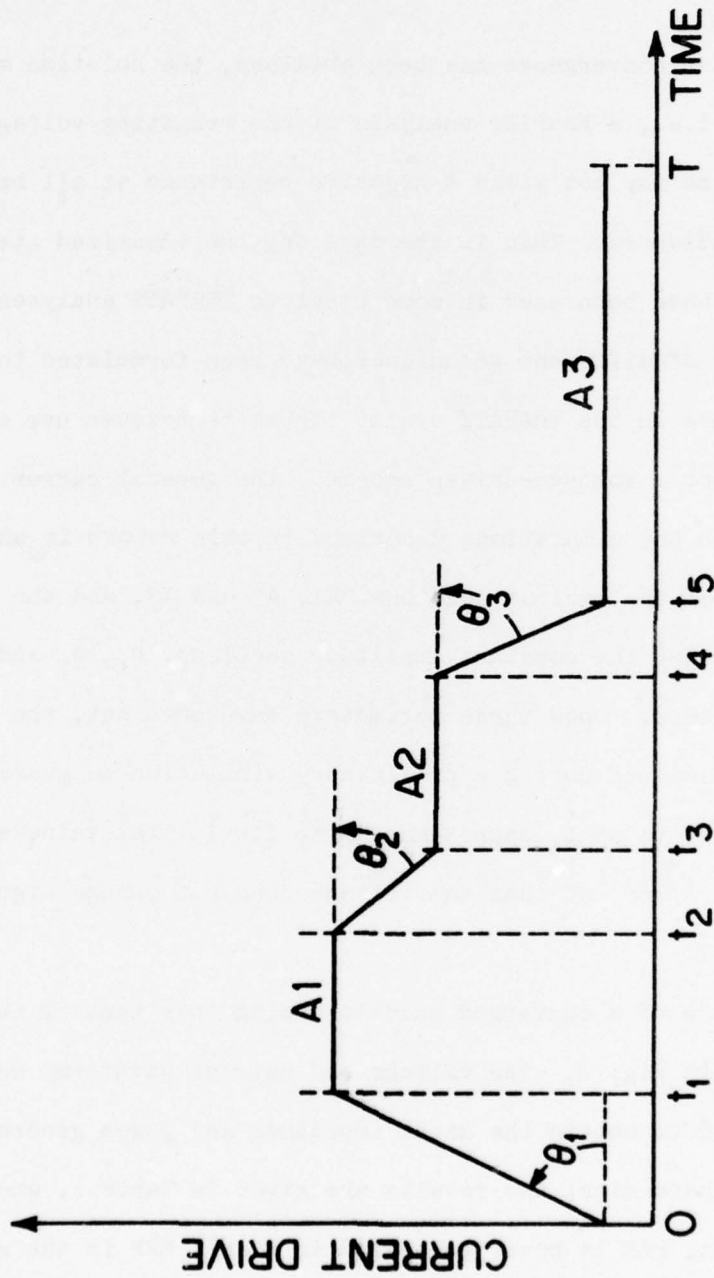


FIG. 1 CURRENT-DRIVE WAVEFORM SHOWING VARIABLE PARAMETERS.

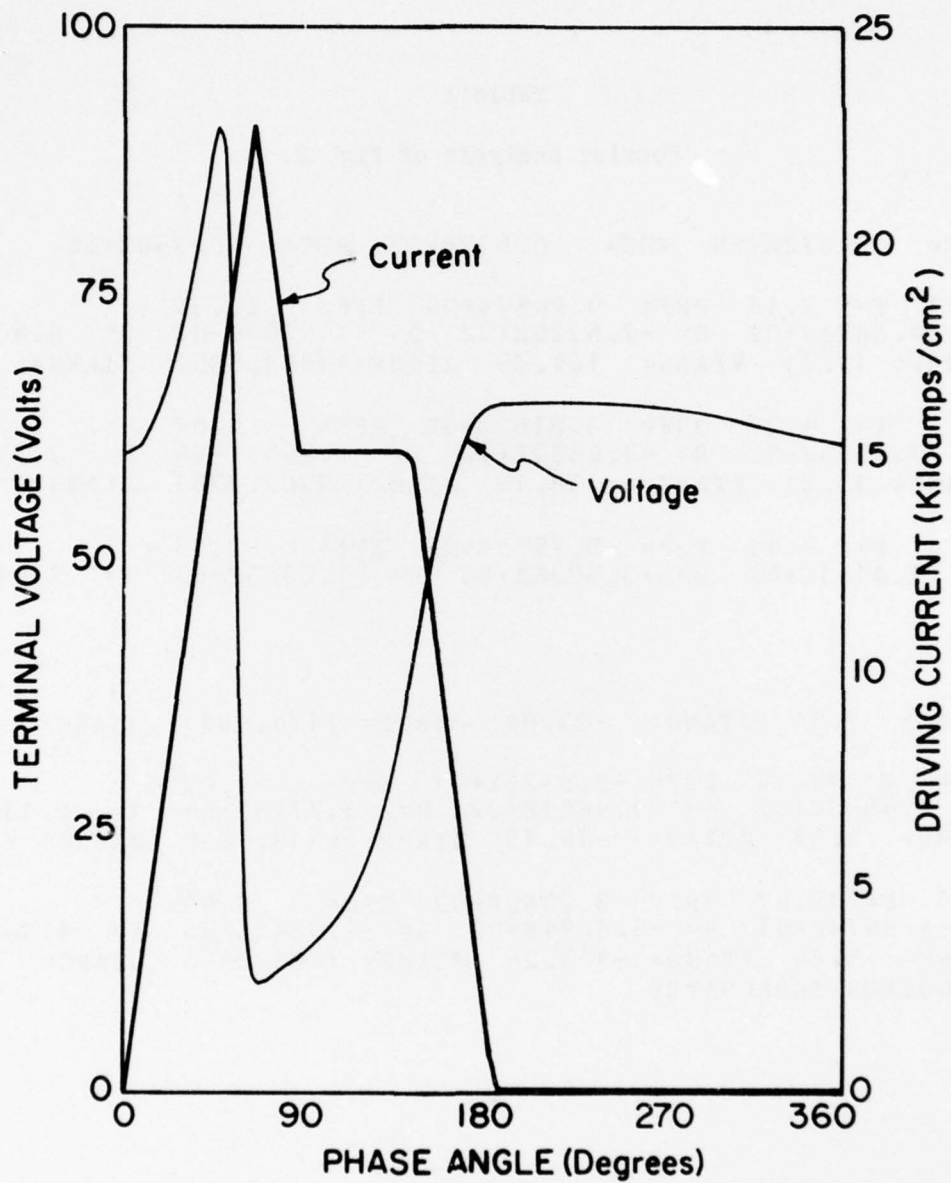


FIG. 2 CURRENT DRIVE AND RESULTING VOLTAGE FOR A CONVERGED SOLUTION.

(Si, 500°K, $f = 3.1$ GHz)

Table 1

Fourier Analysis of Fig. 2.

JDC= 0.672E+04 VDC= 0.532E+02 PDC= 0.358E+06

I= 1 F= 3.13 PRF= 9.4457E+04 EFF= 26.39
G= -4.8628E+02 B= -2.5226E+02 R= -1.6204E-03 X= 8.4058E-04
VTAMP= 19.71 VTANG= 164.39 JIAMP= 11868.5352 JIANG= 20.53

I= 2 F= 6.27 PRF= 1.8152E+04 EFF= 5.07
G= -1.4523E+02 B= -3.6832E+02 R= -9.2650E-04 X= 2.3497E-03
VTAMP= 15.81 VTANG= 58.19 JIAMP= 9362.3281 JIANG= -46.00

I= 3 F= 9.40 PRF= -9.7555E+03 EFF= -2.73
G= 2.0161E+02 B= -3.9226E+02 R= 1.0305E-03 X= 2.0166E-03

VTAMP= 9.04 VTANG= -23.84 JIAMP= 7174.4844 JIANG= -97.79

I= 4 F= 12.54 PRF= -3.8326E+03 EFF= -1.07
G= 2.6592E+02 B= -7.9601E+02 R= 3.7743E-04 X= 1.1302E-03
VTAMP= 5.37 VTANG= -64.13 JIAMP= 6639.4805 JIANG= -141.72

I= 5 F= 15.67 PRF= 3.2060E+02 EFF= 0.09
G= -1.8673E+01 B= -6.8094E+02 R= -4.0241E-05 X= 1.4675E-03
VTAMP= 5.85 VTANG= -103.26 JIAMP= 7005.2500 JIANG= 165.85
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components of terminal voltage and current (less the displacement component) according to the equations

$$VT(I) = VTAMP(I) \sin [\omega t + VTANG(I)]$$

and

$$JT(I) = JIAMP(I) \sin [\omega t + JIAMP(I)] ,$$

where the unit of current is A/cm².

Although this is a converged solution, it does not represent a realistic case because the diode does not exhibit negative resistance at the third and fourth harmonics. A technique for circumventing this difficulty will be described later in the report.

Table 2 lists the results of a Fourier analysis of the voltage and current during the first cycle of simulation after the times t_1 - t_5 were determined so that the voltage recovered at the end of the cycle approximately to the starting value. It is seen that the impedances agree to within approximately 10 percent up to the third harmonic. Evidence from several such comparisons has indicated that the diode can be well characterized up to the third harmonic by a single cycle simulation, and that it is unnecessary to go through the time and expense required to obtain a converged solution, at least as far as the diode impedances are concerned.

For particularly stubborn cases, it was necessary to use a voltage-driven scheme to obtain convergence. This approach is more effective because the diode is much more sensitive to small changes in driving voltage than to changes in driving current, and the convergence process consists of varying some parameter, such as the dc voltage level cycle after cycle. However, this approach introduces new difficulties, some of which are illustrated in Fig. 3. The simulation here was

Table 2

Fourier Analysis of One-Cycle Simulation

Using Current Drive of Fig. 2.

JDC= 0.688E+04 VDC= 0.530E+02 PDC= 0.364E+06

I= 1 F= 3.13 PRF= 9.7827E+04 EFF= 26.84
G= -4.5093E+02 B= -2.7932E+02 R= -1.6027E-03 X= 9.9277E-04
VTAMP= 20.83 VTANG= 161.86 JIAMP= 12312.9297 JIANG= 22.14

I= 2 F= 6.27 PRF= 1.8411E+04 EFF= 5.05
G= -1.3459E+02 B= -3.4525E+02 R= -9.8015E-04 X= 2.5143E-03
VTAMP= 16.54 VTANG= 63.82 JIAMP= 9381.9180 JIANG= -39.90

I= 3 F= 9.40 PRF= -8.9045E+03 EFF= -2.44
G= 2.0227E+02 B= -4.1155E+02 R= -9.6189E-04 X= 1.9571E-03
VTAMP= 9.38 VTANG= -12.30 JIAMP= 7019.0469 JIANG= -86.61

I= 4 F= 12.54 PRF= -1.6090E+03 EFF= -0.44
G= 1.0851E+02 B= -8.3079E+02 R= 1.5458E-04 X= 1.1835E-03
VTAMP= 5.45 VTANG= -41.78 JIAMP= 6790.9492 JIANG= -126.79

I= 5 F= 15.67 PRF= 1.2612E+03 EFF= 0.35
G= -6.6422E+01 B= -6.5327E+02 R= -1.5405E-04 X= 1.5151E-03
VTAMP= 6.16 VTANG= -84.16 JIAMP= 7207.1758 JIANG= -177.42

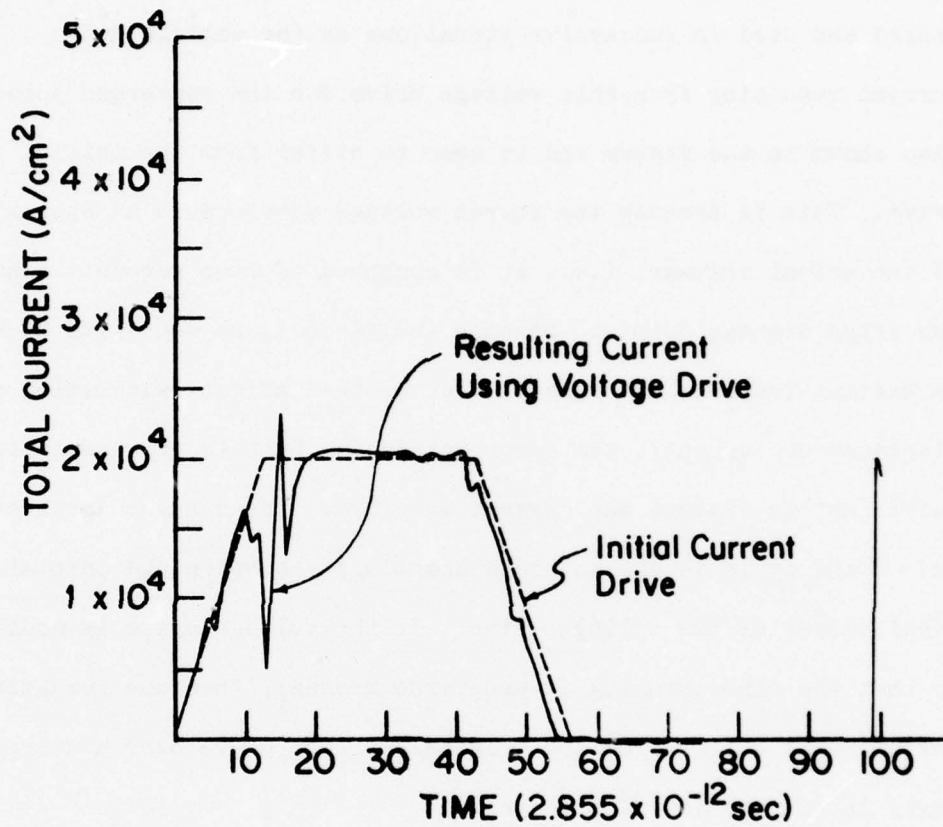


FIG. 3 DISTORTION OF TERMINAL CURRENT WAVEFORM PRODUCED BY A VOLTAGE-DRIVEN SCHEME.

started using a current-driven scheme, where the initial current drive is the step waveform (with finite rise and fall times) shown in the figure. The voltage waveform resulting from this current drive was stored and used in successive iterations as the voltage drive. The current resulting from this voltage drive for the converged solutions is also shown in the figure and is seen to differ from the initial current drive. This is because the stored voltage waveform is an approximation of the actual voltage, i.e., it is composed of line segments connecting the array storage points. Because the diode is so sensitive to voltage variations (especially changes in slope that affect calculation of the displacement current), the error introduced by this representation is sufficient to distort the current waveform. The current spike at the end of the cycle is due to the discontinuity between the initial and final values of the voltage drive. If the voltage drive is modified so that the discontinuity is made more gradual, then the resulting total current will differ from the original current drive over a correspondingly larger portion of the cycle.

Table 3 shows a Fourier analysis of the final converged solution for this case. Table 4 shows the Fourier analysis of the first cycle of simulation for which the stepped current drive was used. Again, good agreement is observed up to the third harmonic; however, these waveforms are unrealistic at the third harmonic because the real part of the impedance at the third harmonic is positive.

On the basis of the above information it was decided to design the amplifier using only the first three harmonics. The results indicated that good characterization of the diode could be obtained using a one cycle simulation at these frequencies. The decision was also

Table 3

Fourier Analysis of Converged Solution of Fig. 3.

O.828E+04 VDC= 0.501E+02 PDC= 0.414E+06									
I= 1	F= 5.50	PRF=	1.1345E+05	EFF=	27.38				
G=	-5.6048E+02	B=	-2.4247E+02	R=	-1.5029E-03	X=	6.5018E-04		
VTAMP=	20.12	VTANG=	162.29	JIAMP=	13374.7813	JIANG=	14.82		
I= 2	F= 7.00	PRF=	1.7978E+04	EFF=	4.34				
G=	-1.2013E+02	B=	-2.5148E+02	R=	-1.5466E-03	X=	3.2376E-03		
VTAMP=	17.30	VTANG=	59.08	JIAMP=	8583.5078	JIANG=	-44.93		
I= 3	F= 10.51	PRF=	-9.3372E+03	EFF=	-2.25				
G=	3.0199E+02	B=	-3.6048E+02	R=	1.3856E-03	X=	1.6303E-03		
VTAMP=	7.86	VTANG=	-5.27	JIAMP=	6033.7266	JIANG=	-72.09		
I= 4	F= 14.01	PRF=	-1.3315E+02	EFF=	-0.03				
G=	5.6273E+00	B=	-6.4078E+02	R=	1.3704E-05	X=	1.5605E-03		
VTAMP=	6.88	VTANG=	-24.53	JIAMP=	7570.8750	JIANG=	-114.24		
I= 5	F= 17.51	PRF=	-8.9120E+02	EFF=	-0.22				
G=	3.7491E+01	B=	-5.1806E+02	R=	1.3896E-04	X=	1.9202E-03		
VTAMP=	6.89	VTANG=	-82.55	JIAMP=	7539.4141	JIANG=	-170.59		

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Table 4

Fourier Analysis of One-Cycle Simulation Using

Initial Current Drive of Fig. 3.

JCC=	0.887E+04	VDC=	0.508E+02	POC=	0.439E+06		
I= 1	F= 3.50	PRF=	1.1754E+05	EFF=	26.95		
G=	-5.8162E+02	B=	-2.4679E+02	R=	-1.4570E-03	X=	6.1822E-04
VTAMP=	20.10	VTANG=	162.44	JIAMP=	13770.0352	JIANG=	14.32
I= 2	F= 7.00	PRF=	1.9692E+04	EFF=	4.52		
G=	-1.3229E+02	B=	-2.7308E+02	R=	-1.4374E-03	X=	2.9664E-03
VTAMP=	17.25	VTANG=	58.90	JIAMP=	8972.6563	JIANG=	-45.75
I= 3	F= 10.51	PRF=	-9.3617E+03	EFF=	-2.15		
G=	3.0235E+02	B=	-3.8949E+02	R=	1.2436E-03	X=	1.6021E-03
VTAMP=	7.87	VTANG=	-9.06	JIAMP=	6249.9000	JIANG=	-73.28
I= 4	F= 14.01	PRF=	5.9207E+02	EFF=	0.14		
G=	-2.4863E+01	B=	-6.7777E+02	R=	-5.4050E-05	X=	1.4734E-03
VTAMP=	6.90	VTANG=	-24.94	JIAMP=	7852.6133	JIANG=	-116.19
I= 5	F= 17.51	PRF=	5.8876E+01	EFF=	0.01		
G=	-2.3491E+00	B=	-5.4452E+02	R=	-7.9224E-06	X=	1.8364E-03
VTAMP=	6.95	VTANG=	-82.61	JIAMP=	7776.9258	JIANG=	-172.73

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motivated by the fact that RCA has successfully designed a TRAPATT oscillator using a three harmonic design approach.⁹

However, before useful design criteria can be determined, the diode must be characterized over the entire design frequency band of the amplifier, ranging from the low end of the fundamental band to the high end of the third harmonic band. To obtain this characterization, the diode must be driven in such a way that negative resistance is exhibited at least for the first three harmonics.

One current drive which does give negative resistance is shown in Fig. 4, along with the resulting voltage. The driving current is triangular shaped and reaches its peak when the voltage is low. A Fourier analysis of this one cycle simulation is given in Table 5. It is seen that negative resistance is exhibited for the first five harmonics. By making the initial rise of the current drive steeper, higher fundamental efficiency can be obtained; the maximum efficiency thus obtained was about 30 percent. This driving current is similar to that experimentally observed by Snapp¹⁰ as illustrated in Fig. 5.

A series of such results were obtained for different frequencies and for different values of capacitance directly in parallel with the diode. Knowing the diode impedance characteristics over a frequency band and the required gain, the external circuit requirements could be determined. The type of circuit used is illustrated in Fig. 6. The power gain of such a reflection amplifier is given by

$$\frac{P_{out}}{P_{in}} = \left| \frac{Y_D - Y_N^*}{Y_D + Y_N} \right|^2, \quad (9)$$

where Y_D is the diode admittance (obtained from analyses like the one

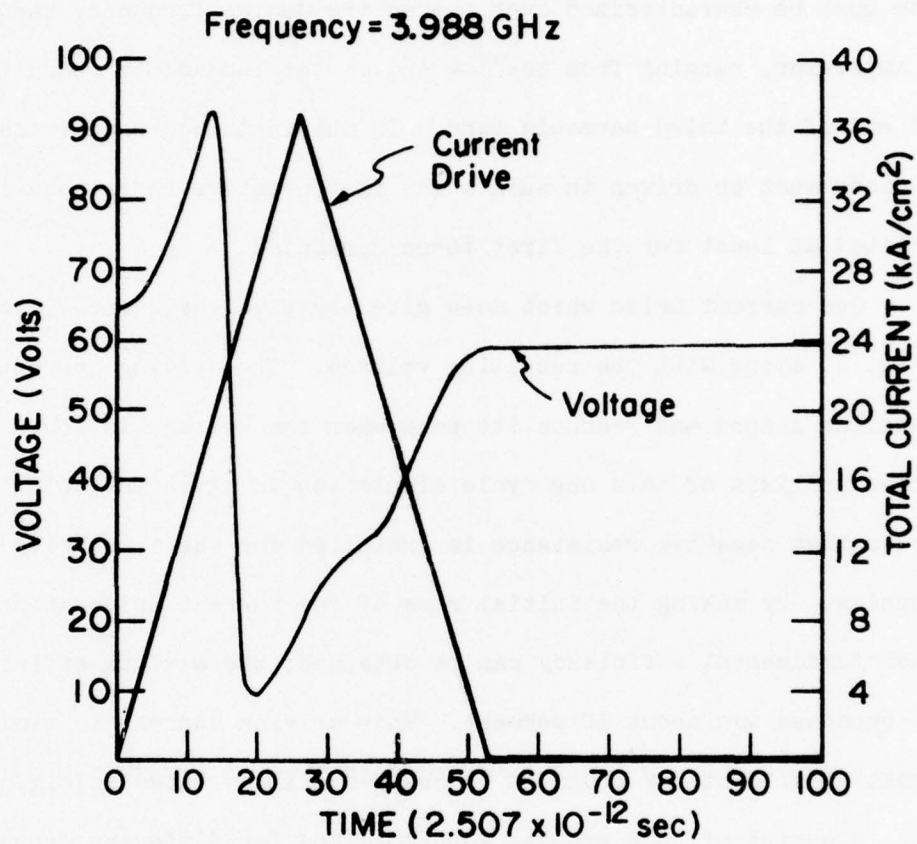


FIG. 4 CURRENT DRIVE AND RESULTING VOLTAGE FOR A ONE-CYCLE SIMULATION THAT EXHIBITS NEGATIVE RESISTANCE AT FIVE HARMONICS.

Table 5
Fourier Analysis of One-Cycle Simulation
of Fig. 4.

~~JCC= 0.102E+05 VDC= 0.523E+02 PDC= 6.532E+06~~

I= 1 F= 3.99 PRF= 1.0467E+05 EFF= 19.69
~~G= -8.9558E+02 B= -6.2667E+02 R= -7.4958E-04 X= 5.2451E-04~~
VTAMP= 15.29 VTANG= 149.43 JIAMP= 17933.9531 JIANG= 9.66

I= 2 F= 7.98 PRF= 4.2243E+04 EFF= 7.95
~~G= -4.1846E+02 B= -4.9560E+02 R= -9.9460E-04 X= 1.1780E-03~~
VTAMP= 14.21 VTANG= 55.71 JIAMP= 12295.1445 JIANG= -63.21

I= 3 F= 11.96 PRF= 5.2005E+03 EFF= 0.98
~~G= -1.2141E+02 B= -3.8760E+02 R= -7.3556E-04 X= 2.3495E-03~~
VTAMP= 9.26 VTANG= -14.08 JIAMP= 7308.8750 JIANG= -112.92

I= 4 F= 15.95 PRF= 5.0835E+02 EFF= 0.10
~~G= -2.2124E+01 B= -5.2525E+02 R= -8.0052E-05 X= 1.9005E-03~~
VTAMP= 6.78 VTANG= -54.42 JIAMP= 7111.4336 JIANG= -145.63

I= 5 F= 19.94 PRF= 4.4519E+02 EFF= 0.08
~~G= -1.9853E+01 B= -5.9704E+02 R= -5.5632E-05 X= 1.6731E-03~~
VTAMP= 6.70 VTANG= -109.77 JIAMP= 8382.2461 JIANG= 159.32

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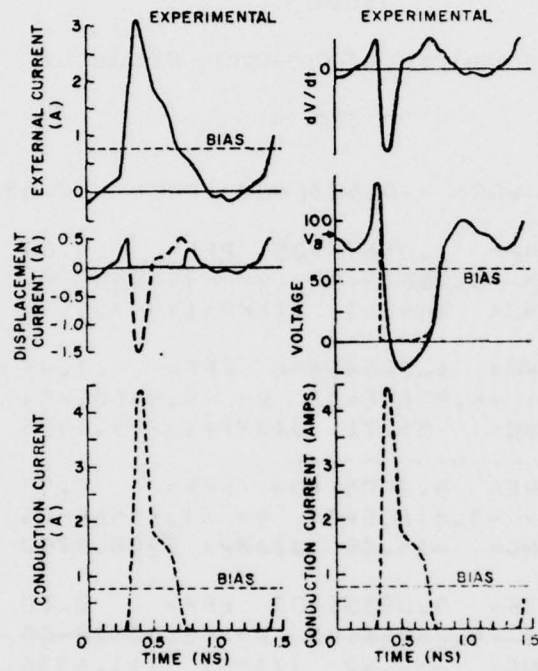


FIG. 5 TRAPPED-PLASMA MODE WAVEFORMS FOR DIODE B OSCILLATING AT

$f_1 = 0.9 \text{ GHz}$ WITH $\eta_1 = 48 \text{ PERCENT.}^{10}$

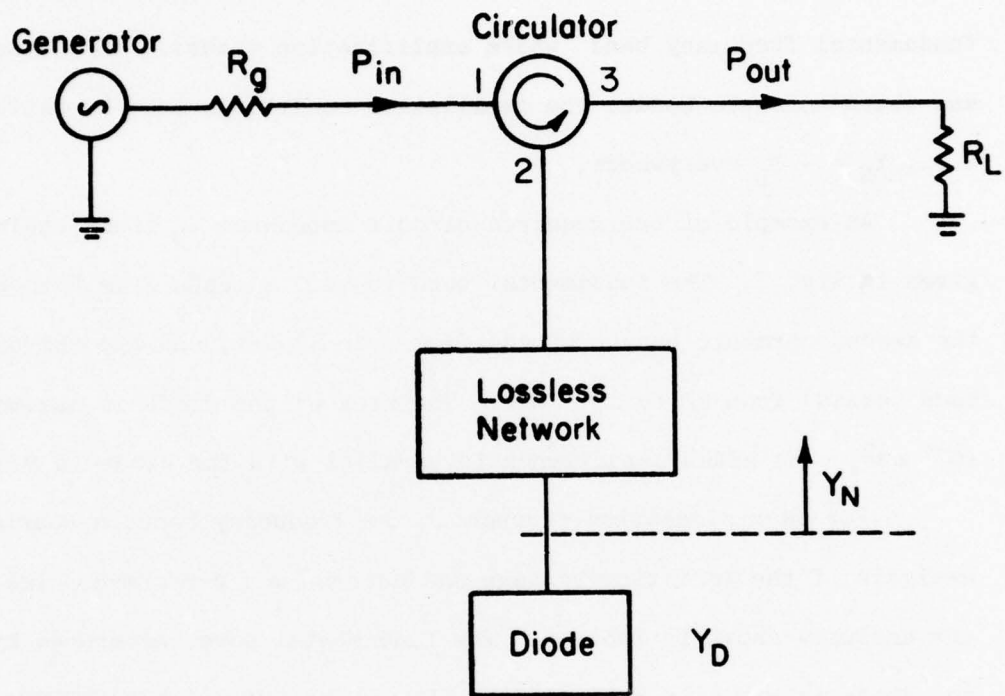


FIG. 6 REFLECTION AMPLIFIER CIRCUIT.

shown in Fig. 4) and Y_N is the admittance of the lossless coupling network terminated in the load resistance. For a desired gain, if Y_D is known for a particular frequency, then a suitable Y_N can be determined by solving the above equation. This specifies the circuit in the fundamental frequency band where amplification occurs. In the second and third harmonic bands, the oscillation conditions must be satisfied, i.e., $Y_N = -Y_D$ everywhere.

An example of the required circuit impedance Z_N thus obtained is given in Fig. 7. The fundamental band (solid) extends from 4 to 6.5 GHz, the second harmonic band (dotted) from 8 to 13 GHz, and the third harmonic band (solid) from 12 to 19.5 GHz. The area of the diode is assumed to be 10^{-4} cm^2 . The added capacitance in parallel with the diode is 0.38 pF.

For each simulation throughout the frequency band, a Fourier analysis of the resulting voltage and current was performed, like the analysis shown in Table 5. The fundamental power generated by the diode is given in Watts/cm² by PRF, where $PRF = (-1/2)(VTAMP)(JIAMP) \cos(VTANG - JIANG)$. To find the actual power generated, PRF is multiplied by the diode area. The fundamental output power vs. frequency calculated in this manner for the amplifier is illustrated in Fig. 8. The diode is a p^+nn^+ structure with a 2- μm n layer, with $n = 8 \times 10^{15} \text{ cm}^{-3}$. The maximum power gain occurs at 5 GHz and is 15 dB. The maximum fundamental efficiency of 28.3 percent occurs at 4.5 GHz.

Figure 9 shows the impedance vs. frequency characteristics for the coaxial oscillator circuit used by Snapp.¹⁰ Comparison with Fig. 7 points out some important qualitative differences between oscillator and amplifier design. The wide variations in impedance of Fig. 9 ensure that the circuit can be tuned to present the most favorable

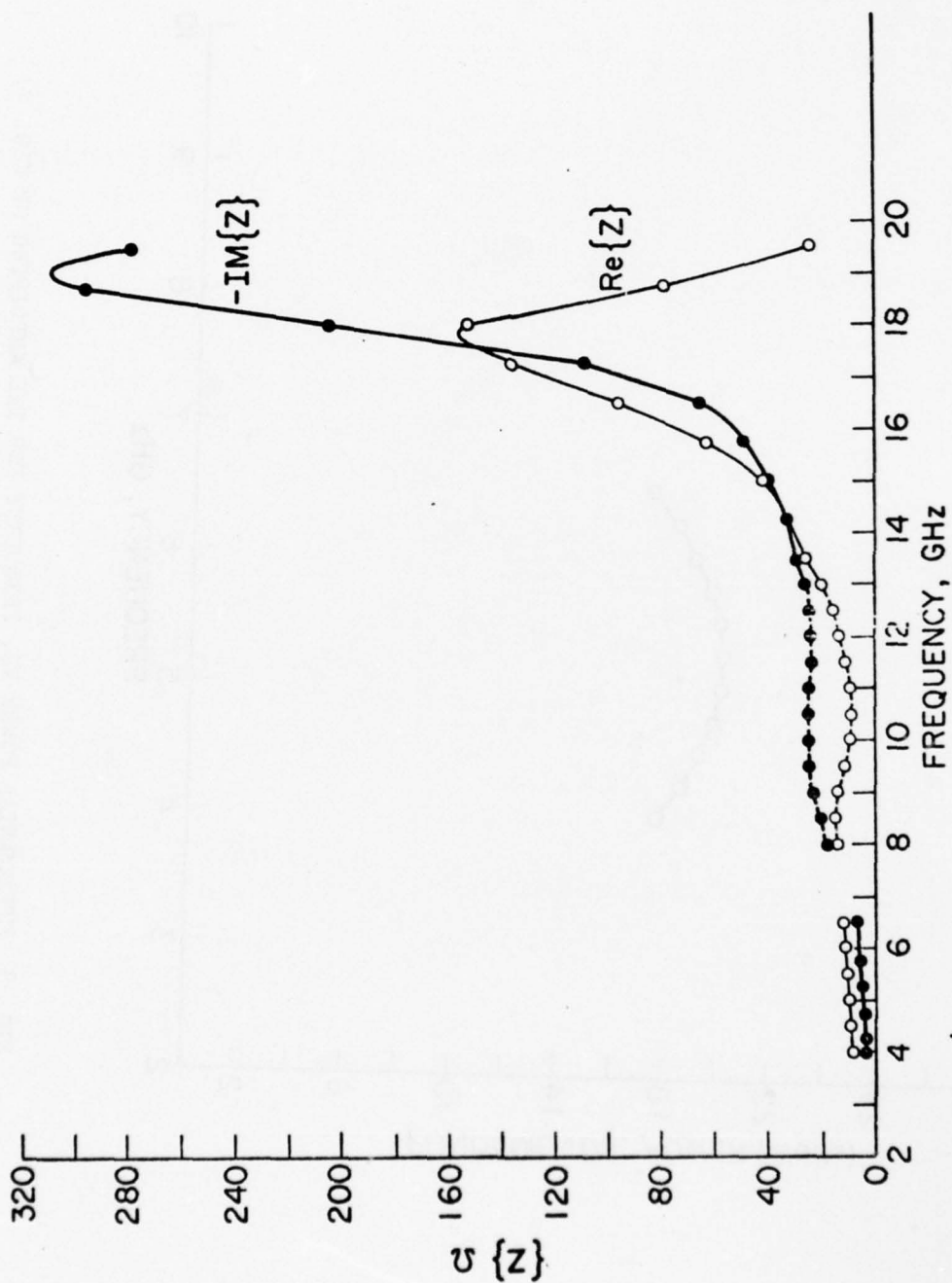


FIG. 7 REQUIRED CIRCUIT IMPEDANCE FOR THE FIRST THREE HARMONIC FREQUENCY BANDS. ($A = 10^{-4} \text{ cm}^2$,

$$C_{\text{added}} = 0.38 \times 10^{-8} \text{ f/cm}, \quad |\Gamma|_{\text{max}}^2 = 15 \text{ dB})$$

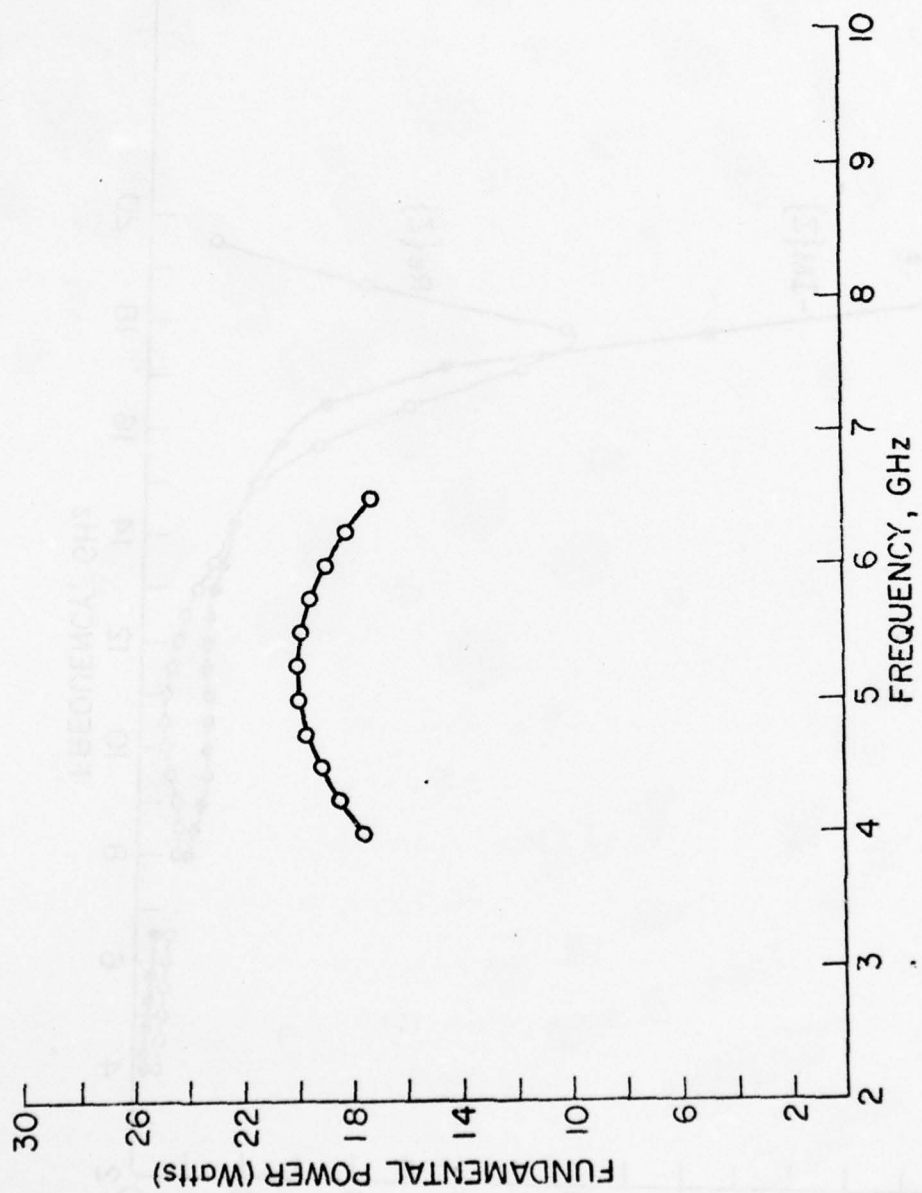


FIG. 8 FUNDAMENTAL POWER VS. FREQUENCY FOR THE AMPLIFIER OF FIG. 7.

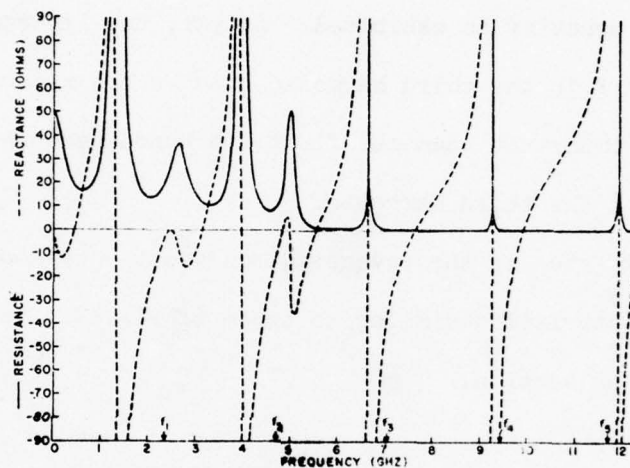


FIG. 9 LOAD IMPEDANCE VS. FREQUENCY FOR DIODE B OSCILLATING IN
 TRAPPED-PLASMA MODE AT $f_1 = 2.35$ GHz WITH $\eta_1 = 37$ PERCENT.
 (THREE 10.2 GHz TUNING SLEEVES -- $Z_{s1} = Z_{s2} = Z_{s3} = 11.3 \Omega$,
 $X_1 = 5.10$ cm, $X_2 = 0.543$ cm, $X_3 = 0.642$ cm)¹⁰

impedance at a set of fixed frequencies $f_1 - f_5$; however, when simultaneous operation over the entire frequency band is envisioned, it is seen that these wide variations tend to prohibit wideband operation. The circuit characteristics in Fig. 7 indicate that the real and imaginary parts should not vary considerably over the fundamental and second harmonic bands; it is only at the high end of the third harmonic band that resonant behavior is exhibited. As yet, the importance of the shape of R and X in the third harmonic band is now known, but it is probably less important than the first two bands because the least power is generated at the third harmonic.

The next step in the investigation was to develop a circuit which realizes characteristics similar to those of Fig. 7. This is discussed in the following section.

III. SYNTHESIS OF CIRCUIT CHARACTERISTICS

The objective of this phase of the investigation was to determine the type of lossless network which would lead to a close approximation of the impedance characteristics of Fig. 7. It was also considered desirable to include some provisions for tuning in the circuit design, since there was no way of knowing how closely the requirements of an actual diode would match the specifications indicated in Fig. 7.

It can be stated that a circuit of the type illustrated in Fig. 10, where a lossless network is placed in series with the load resistance, will never synthesize the required impedance. For this circuit, the imaginary part of the impedance is just the impedance of the lossless network, and it is well known from Foster's reactance theorem that

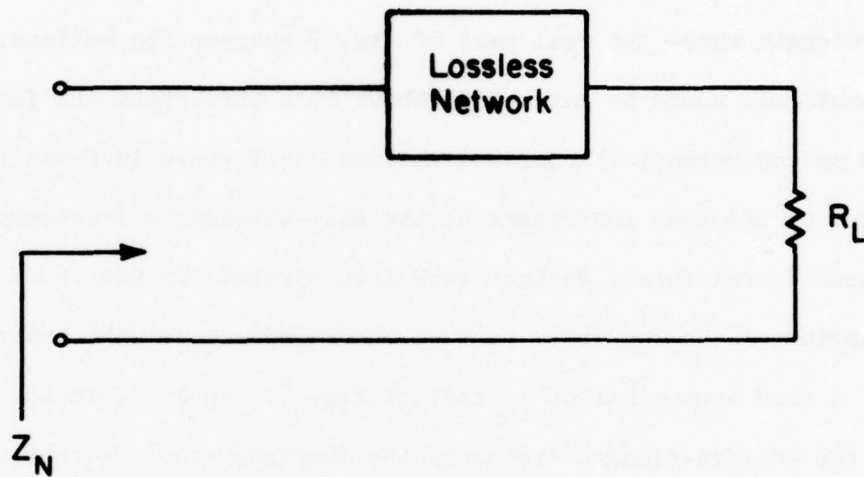


FIG. 10 A CIRCUIT CONFIGURATION WHICH CANNOT SYNTHESIZE THE IMPEDANCE
OF FIG. 7.

$$\frac{\partial x}{\partial \omega} > 0 \quad (10)$$

for a lossless network. However, it is readily apparent from Fig. 7 that $\partial x / \partial \omega < 0$ for most of the frequency range thus violating Foster's reactance theorem.

A circuit which reasonably approximates the real part of Fig. 7 is a stepped impedance transformer whose section length reaches half wavelength where the real part of Fig. 7 reaches its maximum. The transformer would be matched to about 10 Ω throughout the fundamental and second harmonic bands, and the real part would increase to the value of the load resistance at the half-wavelength frequency. Although standard transformer designs were investigated, it was found that the behavior of the imaginary part of the impedance for the transformer was not a good approximation to that of Fig. 7. In fact, in the vicinity of the half wavelength frequency the imaginary part reaches a positive maximum rather than the required minimum impedance. Furthermore, from Foster's reactance theorem it is seen that there does not exist a series lossless network which can be placed between the transformer and the diode to give the correct imaginary part.

Computer-aided design techniques were used to synthesize the required impedance. The circuit consisted of a stepped line of N sections as illustrated in Fig. 11. The objective was to determine the characteristic impedances and section lengths, (Z_1, \dots, Z_N) and (l_1, \dots, l_N) so that $Z_N(j\omega)$ would approximate the impedance of Fig. 7 as closely as possible. If the following error function is formed,

$$E = \sum_{i=1}^{NFREQ} \frac{1}{P} \left| \frac{Z_N(j\omega_i) - Z_S(j\omega_i)}{Z_S(j\omega_i)} \right|^P, \quad (11)$$

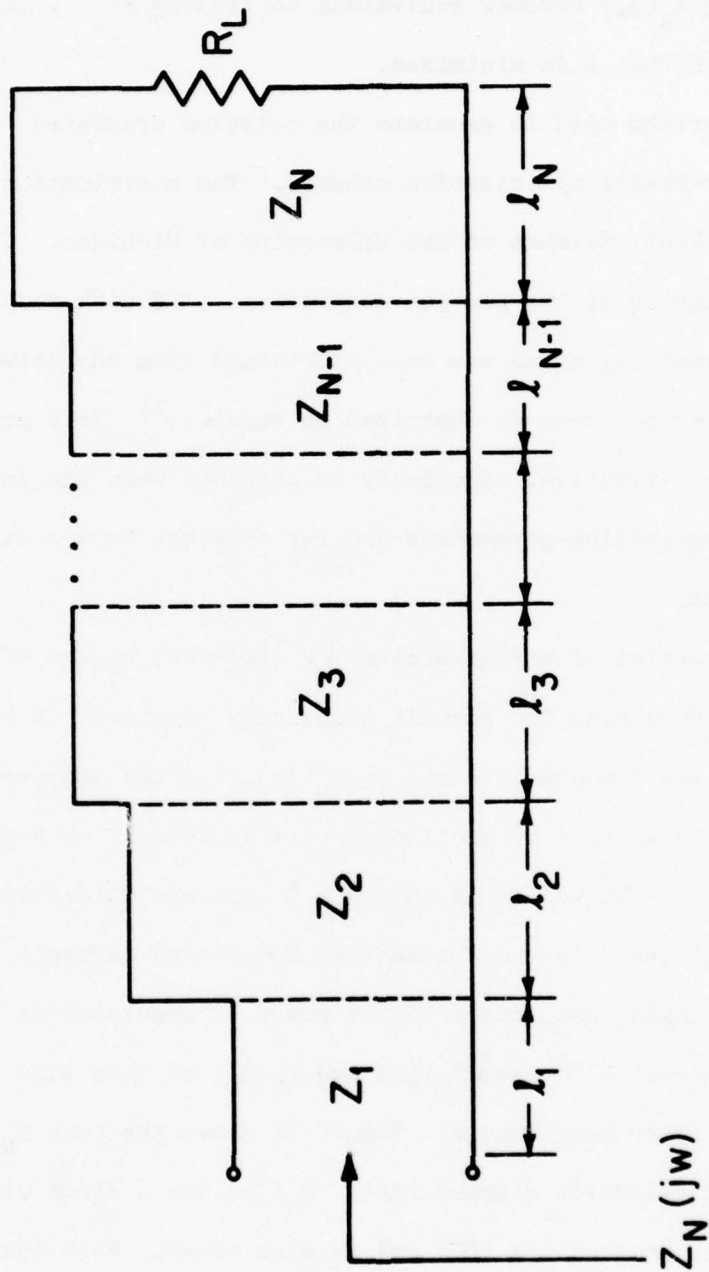


FIG. 11 CIRCUIT CONFIGURATION USED IN THE COMPUTER OPTIMIZATION PROGRAM.

where $Z_S(j\omega)$ is the impedance of Fig. 7 specified at discrete frequencies $(\omega_1, \omega_2, \dots, \omega_{\text{NFREQ}})$, and where p is a positive integer, then the problem of synthesizing $Z_S(j\omega)$ becomes equivalent to finding (Z_1, \dots, Z_N) and (l_1, \dots, l_N) such that E is minimized.

The algorithm used to generate the solution presented here is one of the Fletcher-Powell minimization schemes. The minimization program was written by Prof. Calahan of The University of Michigan. This method requires calculation of the partial derivatives of E with respect to the optimizing parameters, which are easily obtained from one network calculation using the methods described by Bandler.¹¹ This program was found to be very effective, especially in problems when the initial values of the optimizing parameters are far from the values at the error function minimum.

First a series of minimizations for different values of N were carried out to determine the circuit complexity required. N was chosen so that $Z_N(j\omega)$ was reasonably close to $Z_S(j\omega)$, and the improvement obtained by using an $(N + 1)$ section circuit instead of an N -section circuit was minor. It was found that $N = 8$ sections fulfilled these requirements, at least in the fundamental and second harmonic frequency bands. It was hoped that, since little power is generated at the third harmonic, the mismatch between $Z_S(j\omega)$ and $Z_N(j\omega)$ in this band would not impair the amplifier performance. Figure 12 shows the best $Z_N(j\omega)$ obtained for an 8-section stepped line. $Z_S(j\omega)$ for a diode with a 2- μm N layer and area of $2 \times 10^{-4} \text{ cm}^2$ is also shown. Note that the agreement is quite good in the 3 to 8 GHz range for both the real and imaginary parts.

In this minimization procedure, it is entirely possible that the circuit parameters at the error function minimum will turn out to be

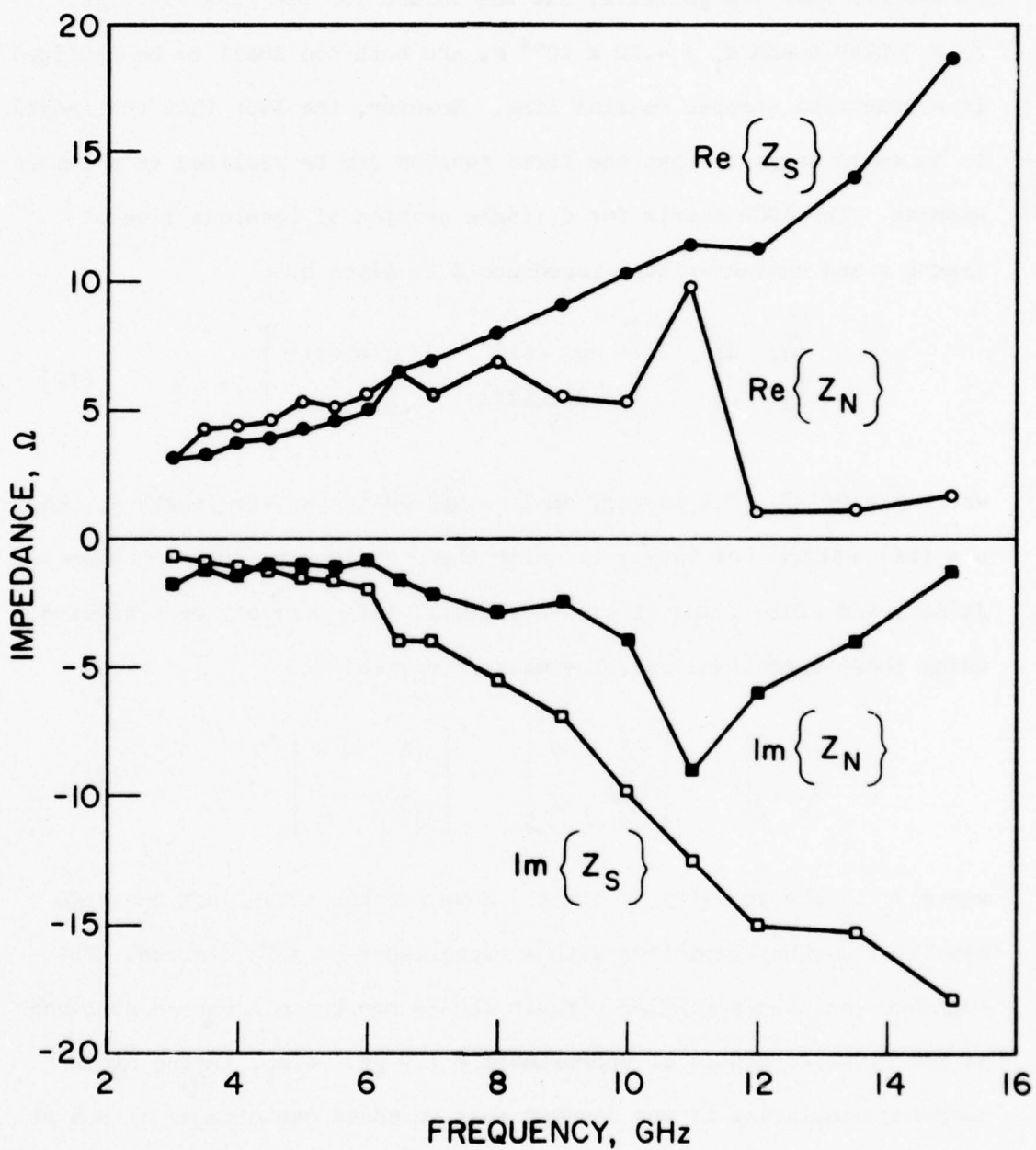


FIG. 12 OPTIMIZED IMPEDANCE OF AN 8-SECTION LINE. (DIODE AREA = $2 \times 10^{-4} \text{ cm}^2$; ADDED CAPACITANCE IN PARALLEL WITH DIODE = 0.5 pF)

unrealizable. For example, one or more of the Z 's or ℓ 's at the solution point could turn out to be negative. For the circuit of Fig. 12 the parameters were all positive, but the values for the first section, $Z = 0.0749 \Omega$ and $\ell_1 = 4.12 \times 10^{-5} \text{ m}$, are both too small to be realized in a practical stepped coaxial line. However, the fact that the length is so small suggests that the first section can be realized as a lumped element. The ABCD matrix for a single section of lossless line of length ℓ and characteristic impedance Z is given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos(\beta\ell) & jZ \sin(\beta\ell) \\ \frac{j \sin(\beta\ell)}{Z} & \cos(\beta\ell) \end{bmatrix}, \quad (12)$$

where $\beta = 2\pi/\lambda$. If ℓ is very small compared to the wavelength λ , then $\sin(\beta\ell) \approx \beta\ell$ and $\cos(\beta\ell) \approx 1$. With these changes the B term becomes $jZ(\beta\ell)$, and since Z and $\beta\ell$ are very small, this term may be neglected. Using these approximations, the matrix becomes

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{j\beta\ell}{Z} & 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{\omega\ell}{jZv_c} & 1 \end{bmatrix}, \quad (13)$$

where v_c is the velocity of light. However, Eq. 13 is just the ABCD matrix of a shunt capacitor with a capacitance of ℓ/Zv_c farads. This suggests that the amplifier circuit should present a shunt capacitance at the diode terminals of approximately 1.9 pF. Also, in the diode computer simulation it was assumed that an added capacitance of 0.5 pF existed at the chip terminals. Thus the circuit should provide a total added capacitance of approximately 2.3 pF.

Figure 13 shows the resulting circuit; Table 6 presents the characteristic impedances and lengths of the sections and also the final error function gradients at the error function minimum point. The meaning of these gradients can be understood referring to Eq. 11 for $E(Z_1, \dots, Z_8 \text{ and } \ell_1, \dots, \ell_8)$. For this particular minimization p was set to 2, and

$$\begin{aligned} \text{GRAD}(Z_i) &= \frac{\partial E}{\partial Z_i} , \\ \text{GRAD}(\ell_i) &= \frac{\partial E}{\partial \ell_i} . \end{aligned} \quad (14)$$

Therefore the gradients are a measure of how much the error function E will change if a single parameter is varied. It is seen from Table 6 that variation of ℓ_1 or Z_1 , or equivalently, variation of the shunt capacitance at the circuit input, will produce a change in E much larger than a corresponding variation in any of the other parameters would produce. This suggests that tuning of the amplifier circuit can best be accomplished by varying the shunt capacitance.

Figure 14 shows the effect on $Z_N(j\omega)$ of decreasing the shunt capacitance from 1.83 to 0.69 pF. Comparison with Fig. 12 shows that decreasing the capacitance tends to make both the real and imaginary parts of $Z_N(j\omega)$ more positive. Figure 15 shows the effect of increasing the shunt capacitance from 1.83 to 2.5 pF. Comparison shows that the effect is mostly to lower the real part of $Z_N(j\omega)$ in the second and third harmonic bands.

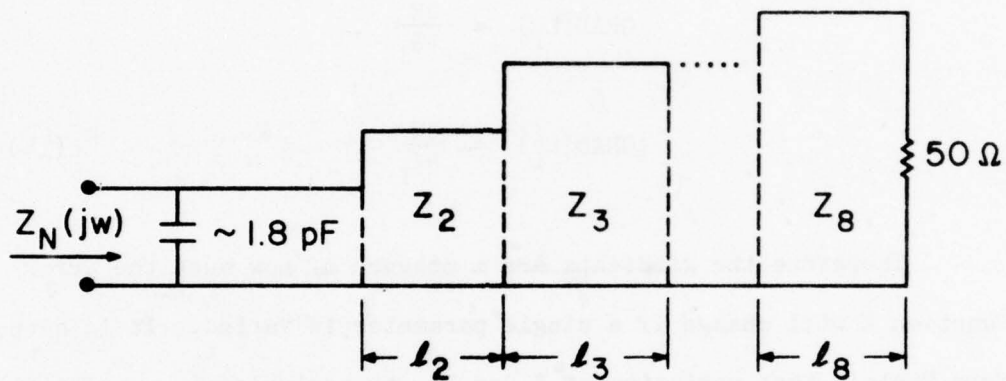


FIG. 13 AMPLIFIER CIRCUIT USING A LUMPED CAPACITOR TO REALIZE THE FIRST SECTION.

Table 6

Circuit Parameters and Gradients at the Error Function Minimum.

i	$Z_i (\Omega)$	$\text{GRAD}(Z_i)$	$\ell_i (\text{m})$	$\text{GRAD}(\ell_i)$
1	7.49×10^{-2}	- 0.542	4.12×10^{-5}	988
2	7.35	3.36×10^{-3}	1.38×10^{-2}	8.49
3	12.8	- 1.50×10^{-3}	1.06×10^{-2}	- 0.411
4	20.3	- 1.86×10^{-3}	1.20×10^{-2}	- 2.18
5	25.8	- 5.67×10^{-3}	1.43×10^{-2}	- 1.38
6	28.8	3.99×10^{-3}	1.42×10^{-2}	- 3.65
7	33.9	9.34×10^{-4}	1.16×10^{-2}	- 2.07
8	42.1	7.20×10^{-4}	1.26×10^{-2}	- 5.92

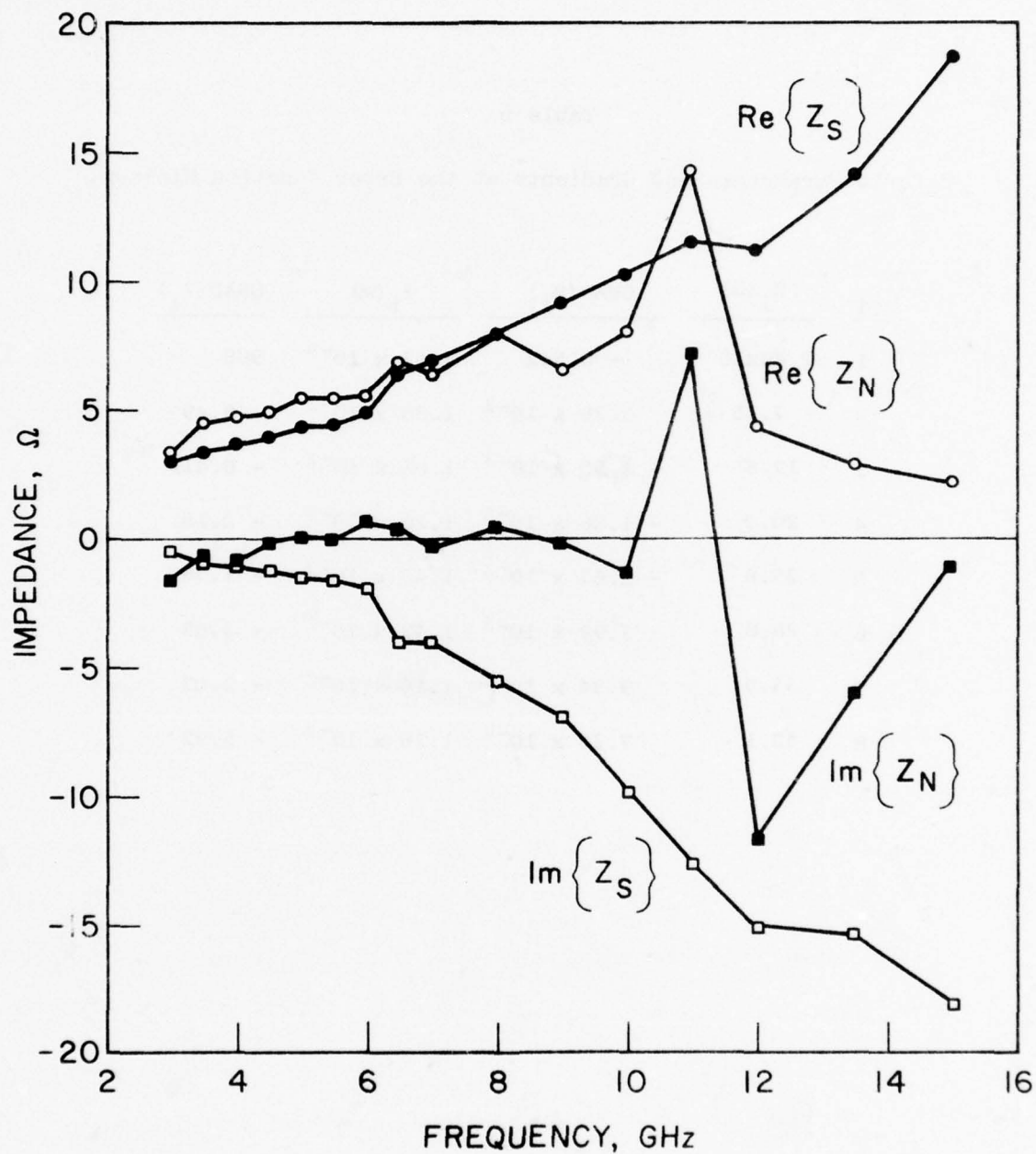


FIG. 14 CIRCUIT IMPEDANCE WITH THE SHUNT CAPACITOR REDUCED TO 0.69 pF.

(DIODE AREA = $2 \times 10^{-4} \text{ cm}^2$; ADDED CAPACITANCE IN PARALLEL WITH DIODE = 0.5 pF)

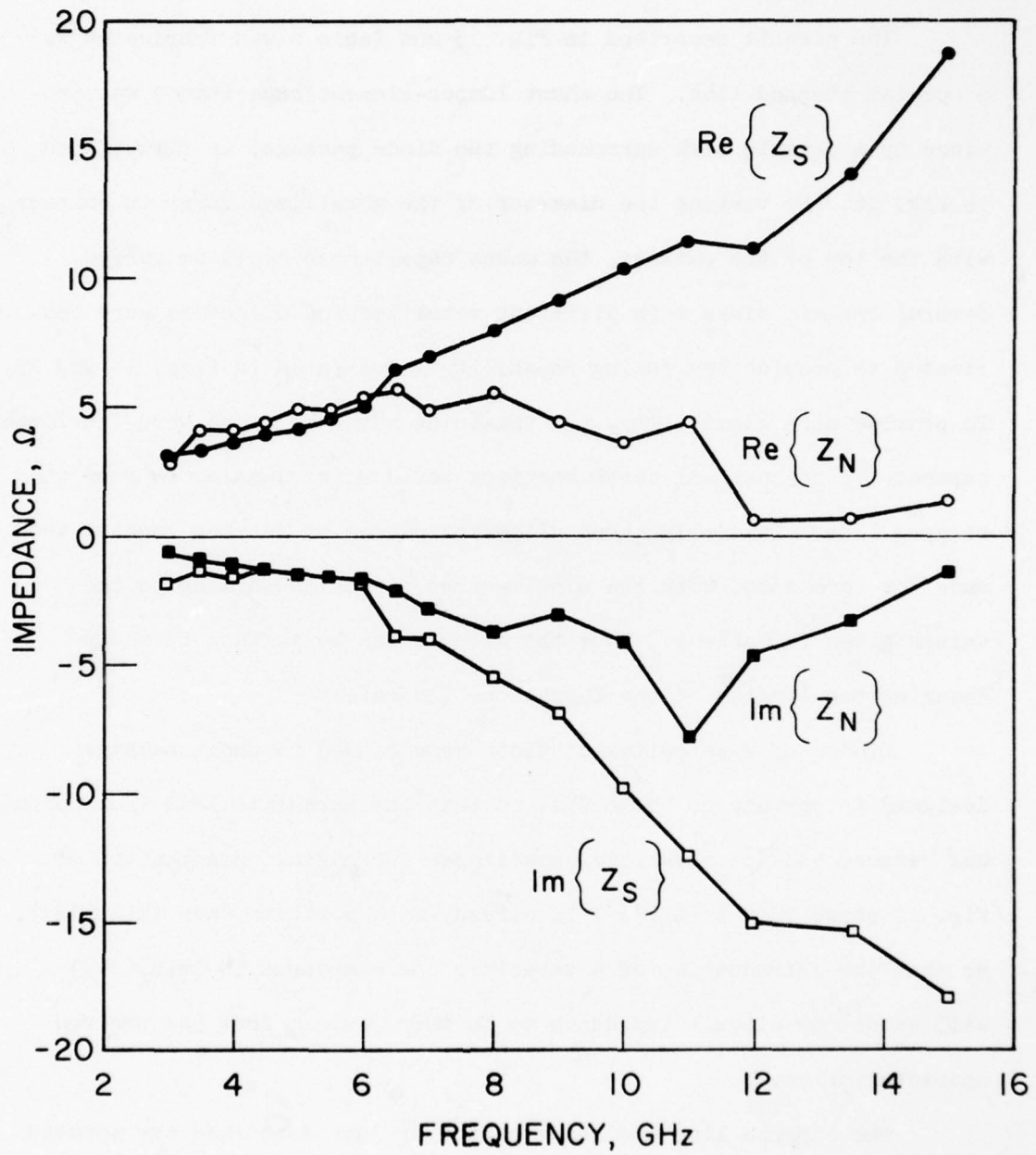


FIG. 15 CIRCUIT IMPEDANCE WITH THE SHUNT CAPACITOR INCREASED TO 2.5 pF.
 (DIODE AREA = $2 \times 10^{-4} \text{ cm}^2$; ADDED CAPACITANCE IN PARALLEL WITH
 DIODE = 0.5 pF)

IV. CONSTRUCTION AND TESTING OF THE CIRCUIT

The circuit described in Fig. 13 and Table 6 was fabricated as a coaxial stepped line. The shunt lumped-element capacitance was provided by a ceramic disk surrounding the diode package, as illustrated in Fig. 16. By varying the diameter of the metallized layer in contact with the top of the package, the shunt capacitance could be varied. Several ceramic disks with different metallization diameters were fabricated to provide the tuning capability illustrated in Figs. 14 and 15. To provide more flexibility, the remaining seven sections were fabricated separately, so that all seven sections could slide together to form the stepped line. Initially three different pieces of varying lengths were made for each step, with the middle-sized pieces conforming to the values given in Table 5. Thus the circuit can be further tuned by changing the lengths of the 7 sections separately.

Diodes of 2- μ m epitaxial width were bonded in small packages designed to operate up to 30 GHz, so that the parasitic lead inductance was reduced and the parasitic capacitance increased. Examination of Fig. 12 shows that $\text{Im}\{Z_N(j\omega)\}$ is already more positive than $\text{Im}\{Z_S(j\omega)\}$, so that the introduction of a parasitic $j\omega L$ component to $\text{Im}\{Z_N(j\omega)\}$ will cause the circuit impedance to further deviate from the desired characteristics.

The stepped line and shunt capacitor just described are located in the "lossless network" box of the reflection amplifier circuit in Fig. 6. Since in the design of this network a 50- Ω termination was assumed, it is important that the circulator appears as 50 Ω at port 2 throughout the frequency band. Unfortunately, circulators are designed to be matched over a one octave bandwidth at best. This suggests

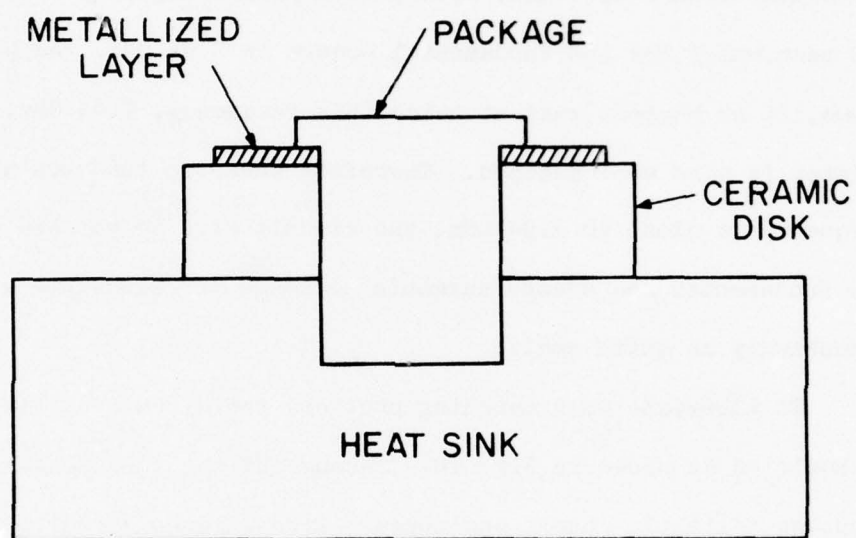


FIG. 16 REALIZATION OF THE SHUNT CAPACITOR IN THE COAXIAL LINE.

that, if the circulator is matched throughout the fundamental band, then it is not possible to obtain a match at the second or third harmonic except at certain isolated frequencies in the bands where the circulator impedance happens to fall near the center of the Smith chart.

Figure 17 shows the input impedance at port 2 of an S-band circulator from 2 to 4 GHz, with 50- Ω terminations on ports 1 and 3. The best match for the fundamental occurs at 3.94 GHz. As Fig. 18 shows, it so happens that at twice this frequency, 7.88 GHz, the circulator is also well matched. Therefore when the fundamental frequency is close to 3.94 GHz, the circuit will be matched at the fundamental and second harmonic although the bandwidth will undoubtedly be quite small.

To alleviate this matching problem, the circuit of Fig. 6 could be modified as shown in Fig. 19. Throughout the fundamental band, the highpass filter is cutoff and appears like an open circuit; therefore the fundamental frequency sees the nearly 50- Ω input impedance at port 2 of the circulator through the lowpass filter. Frequencies at the second and third harmonic bands are blocked by the lowpass filter which is cutoff and appears as an open circuit. These higher frequencies are matched to 50 Ω through the highpass filter.

The coaxial stepped line was tested using the configuration of Fig. 6, i.e., without the increased matching capability which would be provided by the circuit of Fig. 19. Many different combinations of section lengths and ceramic disk metalization diameter were tried but neither amplification nor oscillation was observed for any of these combinations.

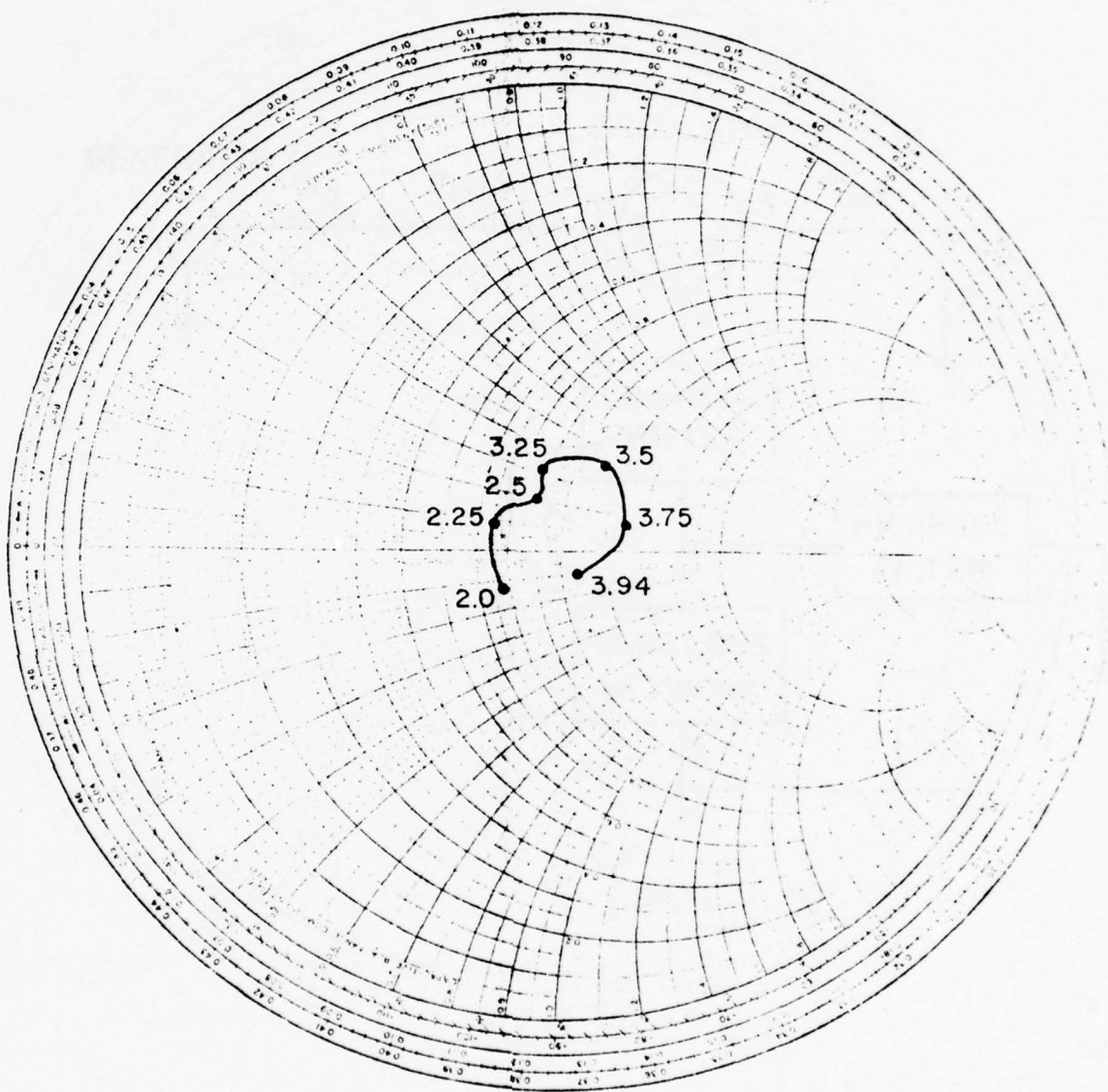


FIG. 17 CIRCULATOR IMPEDANCE AT PORT 2 FROM 2 TO 4 GHz WITH PORTS
1 AND 3 TERMINATED IN 50 Ω .

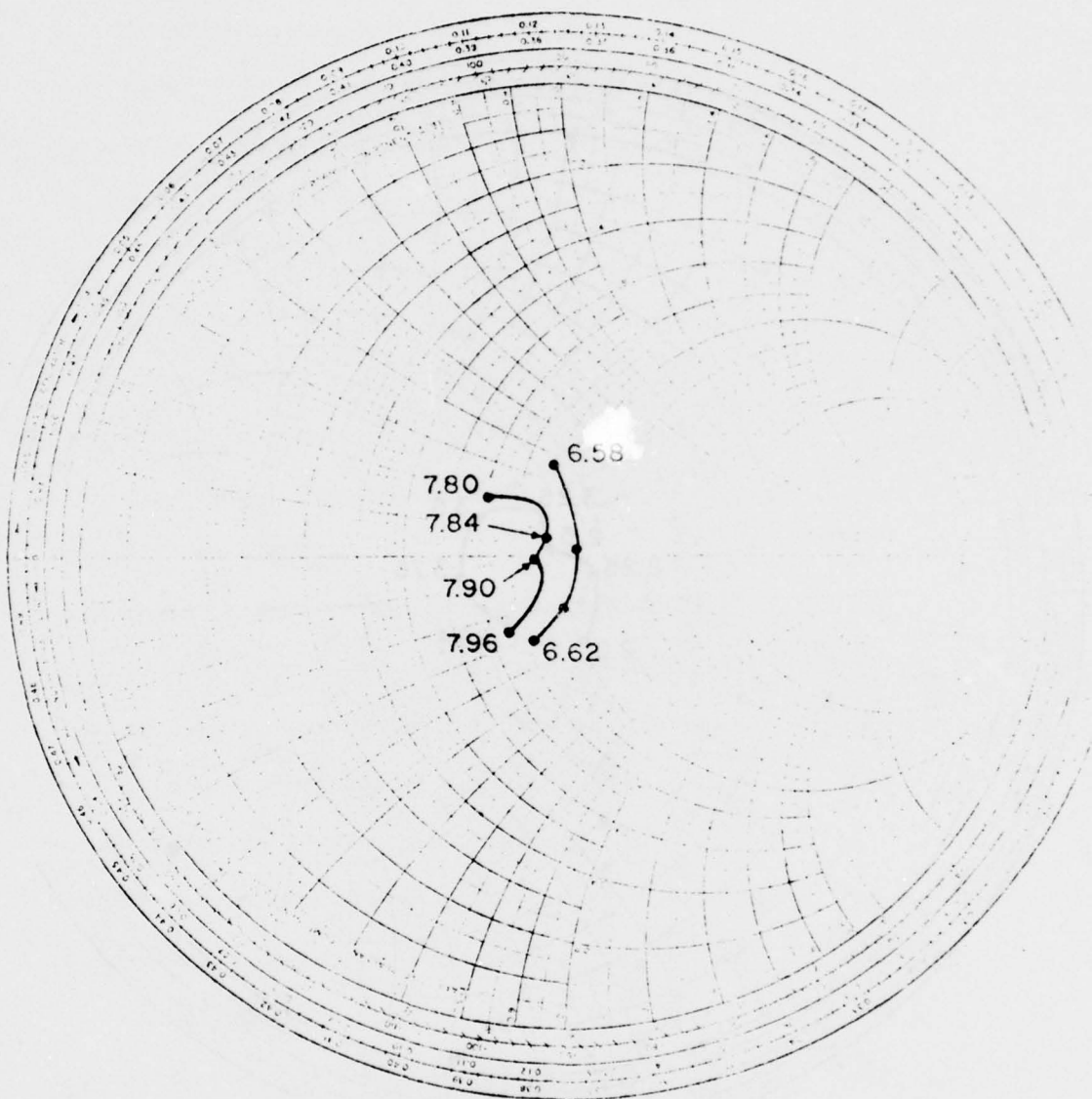


FIG. 18 CIRCULATE IMPEDANCE AT PORT 2 IN THE SECOND HARMONIC BAND
WITH PORTS 1 AND 3 TERMINATED IN 50Ω .

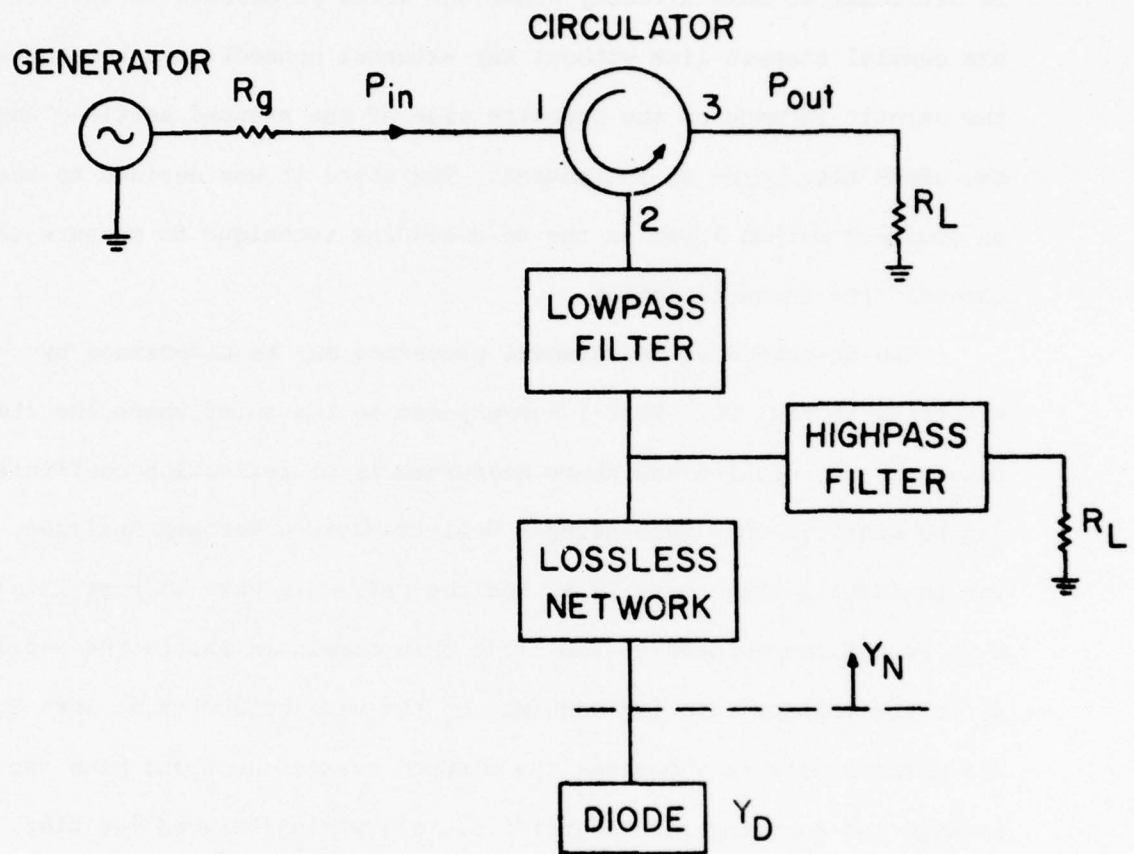


FIG. 19 MODIFIED REFLECTION AMPLIFIER CIRCUIT.

To evaluate this problem, it was decided to measure the impedance vs. frequency characteristics of the stepped line, as determined by looking back into the circuit from the diode chip. This measurement is difficult to make directly since the diode is mounted at the end of the coaxial stepped line without any external connections; contact with the circuit is made on the opposite side of the stepped sections where the diode bias pulse is introduced. Therefore it was decided to use an indirect method known as the de-embedding technique to measure the coaxial line characteristics.

The de-embedding measurement procedure may be understood by referring to Fig. 20. Port 1 corresponds to the point where the diode bias pulse is applied and where measurements of reflection coefficient can be made, in this case using a Hewlett-Packard Network Analyzer. The incident voltage wave is a_0 and the reflected wave at port 1 is b_0 . Port 2 corresponds to the diode chip terminals inside the package; a_1 is the voltage wave incident and b_1 the wave reflected at port 2. The unknown network comprises the stepped coaxial sections plus the package and mounting parameters; i.e., everything between the bias input at 1 and the diode chip at 2. The objective is to determine the impedance seen by the diode chip, looking in at port 2, when the intervening network is terminated at port 1 with 50Ω (this termination assumes that the circulator shown in Fig. 6 looks like 50Ω at input 2). However, it is possible only to measure the reflection coefficient looking in at port 1 and not at port 2. The de-embedding technique requires that three measurements be made at port 1: Γ_{m1} , Γ_{m2} , and Γ_{m3} . For each of these measurements a different known terminating impedance Z_T is attached at port 2; i.e., the measurement

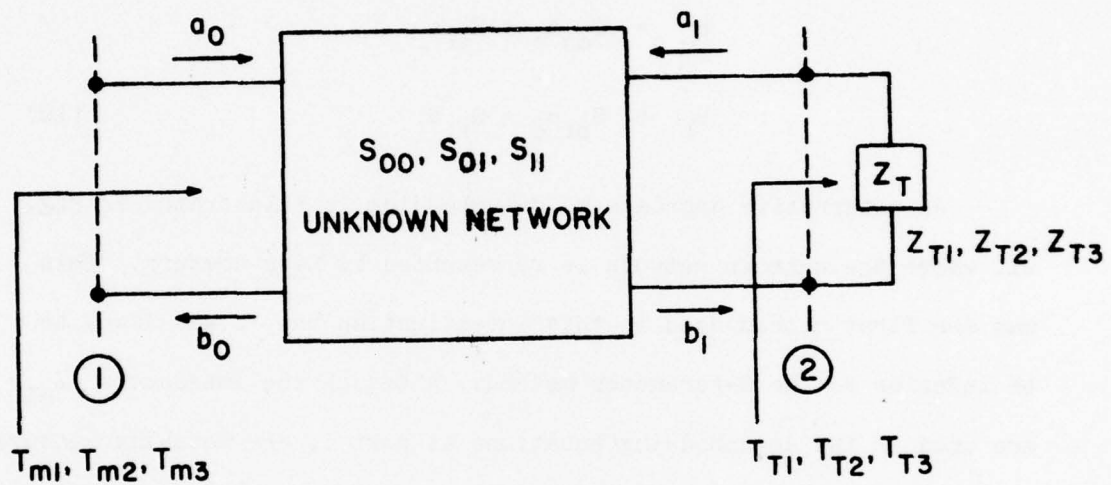


FIG. 20 ILLUSTRATION OF THE DE-EMBEDDING MEASUREMENT TECHNIQUE;
S-PARAMETER METHOD.

Γ_{mi} is taken with the termination Z_{Ti} attached. From Fig. 20, it is seen that

$$\Gamma_{mi} = \frac{b_o}{a_o}, \quad \Gamma_{Ti} = \frac{a_1}{b_1} = \frac{Z_{Ti} - Z_o}{Z_{Ti} + Z_o}, \quad i = 1, 2, 3. \quad (15)$$

The unknown network is characterized by the equations

$$\begin{aligned} b_o &= S_{oo}a_o + S_{ol}a_1, \\ b_1 &= S_{ol}a_o + S_{ll}a_1. \end{aligned} \quad (16)$$

An alternative approach to de-embedding is illustrated in Fig. 21, where the unknown network is represented by Z-parameters. This was the first method used in this investigation but it was found to be inferior to the S-parameter method. Although the impedances (Z_{mi}) are used in the de-embedding equations at port 1, one actually measures the Γ_{mi} 's as before, hence requiring the introduction of the following transformation:

$$Z_{mi} = Z_o \frac{1 + \Gamma_{mi}}{1 - \Gamma_{mi}}. \quad (17)$$

It is seen that if Γ_{mi} approaches 1, considerable numerical error may be introduced by this transformation.

From Fig. 20, it is apparent that

$$\Gamma_{mi} = S_{oo} - \frac{S_{ol}^2 \Gamma_{Ti}}{S_{ll} \Gamma_{Ti} - 1}, \quad i = 1, 2, 3, \quad (18)$$

and from Fig. 21,

$$Z_{mi} = Z_{ll} - \frac{Z_{l2}^2}{Z_{22} + Z_{Ti}}, \quad i = 1, 2, 3. \quad (19)$$

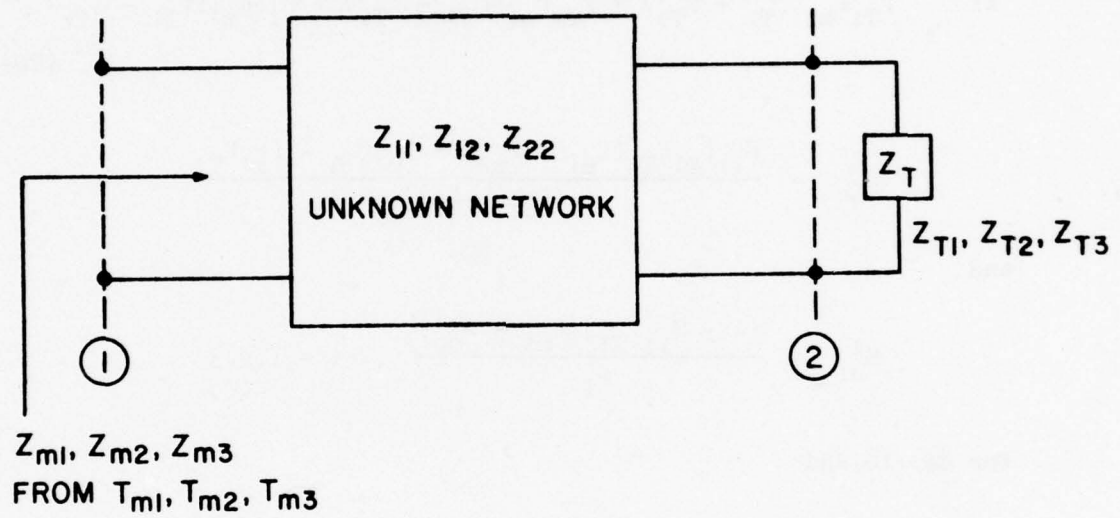


FIG. 21 THE DE-EMBEDDING MEASUREMENT TECHNIQUE; Z-PARAMETER METHOD.

In Eqs. 18 and 19, the Γ_{mi} 's (and hence the Z_{mi} 's) are known from measurement and the Γ_{Ti} 's and Z_{Ti} 's are assumed known; therefore the unknowns are the three S-parameters in Eq. 18 and the three Z-parameters in Eq. 19. Solving for these unknowns yields

$$S_{11} = \frac{\Gamma_{m1}(\Gamma_{T2} - \Gamma_{T3}) + \Gamma_{m2}(\Gamma_{T3} - \Gamma_{T1}) + \Gamma_{m3}(\Gamma_{T1} - \Gamma_{T2})}{\Gamma_{T1}\Gamma_{m1}(\Gamma_{T2} - \Gamma_{T3}) + \Gamma_{T2}\Gamma_{m2}(\Gamma_{T3} - \Gamma_{T1}) + \Gamma_{T3}\Gamma_{m3}(\Gamma_{T1} - \Gamma_{T2})}, \quad (20)$$

$$S_{oo} = \frac{S_{11}\Gamma_{T1}\Gamma_{T2}(\Gamma_{m1} - \Gamma_{m2}) + \Gamma_{m2}\Gamma_{T1} - \Gamma_{m1}\Gamma_{T2}}{(\Gamma_{T1} - \Gamma_{T2})},$$

and

$$S_{oi}^2 = \frac{(1 - S_{11}\Gamma_{Ti})(\Gamma_{mi} - S_{oo})}{\Gamma_i}, \quad i = 1, 2, 3$$

for Eq. 18 and

$$Z_{11} = \frac{(Z_{m1} - Z_{m3})(Z_{m1}Z_{T1} - Z_{m2}Z_{T2}) - (Z_{m1} - Z_{m2})(Z_{m1}Z_{T1} - Z_{m3}Z_{T3})}{(Z_{m1} - Z_{m3})(Z_{T1} - Z_{T2}) - (Z_{m1} - Z_{m2})(Z_{T1} - Z_{T3})},$$

$$Z_{22} = \frac{Z_{m2}Z_{T2} - Z_{m1}Z_{T1} + Z_{11}(Z_{T1} - Z_{T2})}{Z_{m1} - Z_{m2}}, \quad (21)$$

and

$$Z_{12}^2 = (Z_{11} - Z_{m1})(Z_{22} + Z_{T1}), \quad i = 1, 2, 3$$

for Eq. 19.

In this way the S or Z parameters of the network intervening between the measurement port and the diode chip were found. In order to obtain the three known terminating impedances Z_T , a TRAPATT diode was used which was reversed biased below breakdown, so that it behaved

as a varactor. Three different bias voltages were used, for each of which the diode capacitance was known from previous C-V measurements, and the diode series resistance was estimated based on the doping profile. Once the Z_{T1} 's (and Γ_{T1} 's) were known, the measurement of Γ_{m1} (and Z_{m1}) at each bias voltage yielded sufficient information to solve for the S parameters according to Eq. 20, or the Z-parameters according to Eq. 21. The resulting network contains all elements between the measurement port and the diode chip; i.e., the bias T, the stepped coaxial sections, the ceramic disk surrounding the package, the package parasitics and any other elements which might be included in the circuit.

After the S (or Z) parameters were obtained, the impedance which the chip would see if port 1 were terminated in 50Ω ($a_0 = 0$) was obtained from

$$Z = Z_0 \frac{1 + S_{11}}{1 - S_{11}}$$

or

$$Z = Z_{22} - \frac{Z_{12}^2}{Z_{11} + 50} \quad (22)$$

Figure 22 shows the first de-embedding results for the case where the stepped coaxial sections and the ceramic disk have been removed; also a larger (S-4) package was used. The only element in the coaxial line besides the bias T, necessary to set the varactor bias, was a small dielectric support to properly position the center conductor. The impedance plotted is the impedance which would be presented to the chip if the empty cavity were terminated in 50Ω . Z_{m1} and Z_{m2} were separate measurements performed on different days to test repeatability.

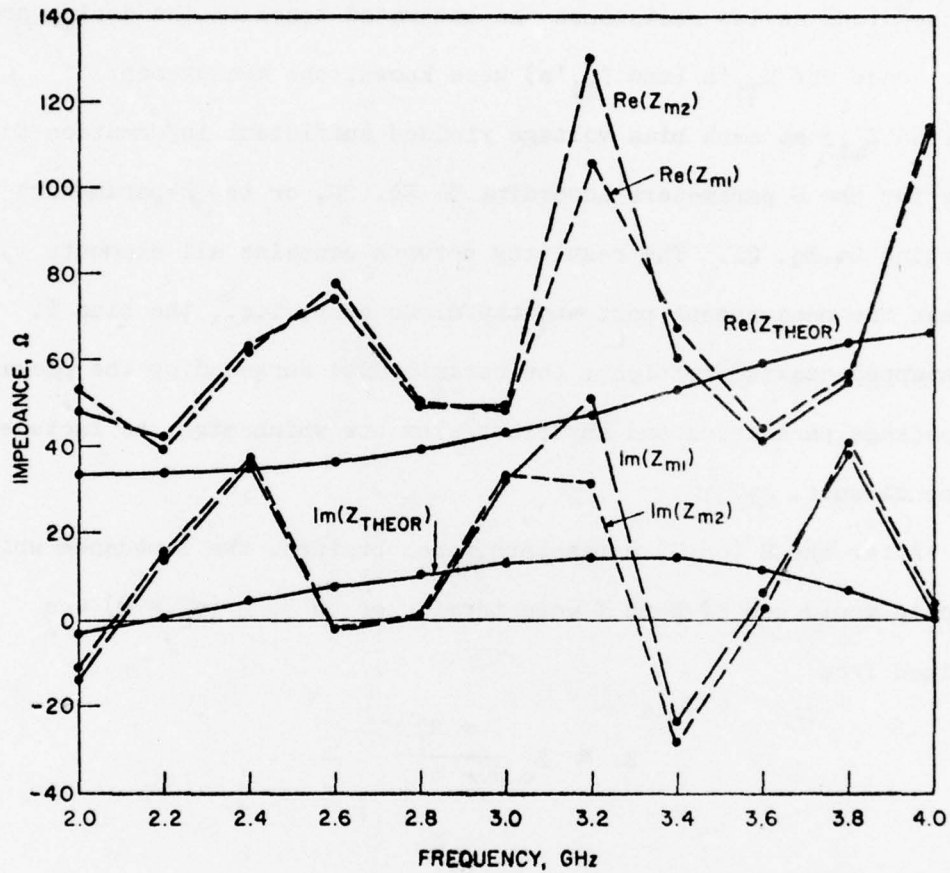


FIG. 22 MEASURED AND THEORETICALLY EXPECTED IMPEDANCE FOR EMPTY COAXIAL LINE WITH NO ERROR CORRECTION.

The Z-parameter algorithm corresponding to Fig. 21 was used for these measurements. Z_{THEOR} is the impedance one would expect to see for the empty cavity assuming the bias T is well matched; the circuit used to calculate Z_{THEOR} is shown in Fig. 23.

There is evidently considerable discrepancy between measured and theoretical results in Fig. 22. In addition, the peak-to-peak variation in measured data is much greater than would be expected for such a simple circuit. At this point in the investigation, two reasons for this discrepancy were proposed. The first was related to the transformation of Eq. 17. The Γ_{mi} 's are for a nearly lossless circuit, since the only loss is the diode resistance and the loss in the empty coaxial line, and it is precisely when $|\Gamma_{\text{mi}}|$ approaches unity that one is likely to have difficulty with this transformation. The second reason was the error introduced by the network analyzer system.

To remedy the first source of error, it was decided to convert to the S-parameter algorithm so that the transformation in Eq. 18 was avoided. As for the second difficulty, a network analyzer error correction procedure was formulated. This correction procedure uses the de-embedding technique illustrated in Fig. 20; the S-parameters of the unknown network now represent the errors introduced by the network analyzer, and it is assumed that these errors are adequately represented by a linear, reciprocal two port. Port 2 of Fig. 20 is now the physical point where an unknown is connected for network analyzer reflection coefficient measurement. Therefore the Γ_{Ti} 's are the actual reflection coefficients of three known, standard terminations, e.g., a short, open, and matched 50 Ω load. The reflection coefficients Γ_{mi} at port 1 are the readings displayed by the network

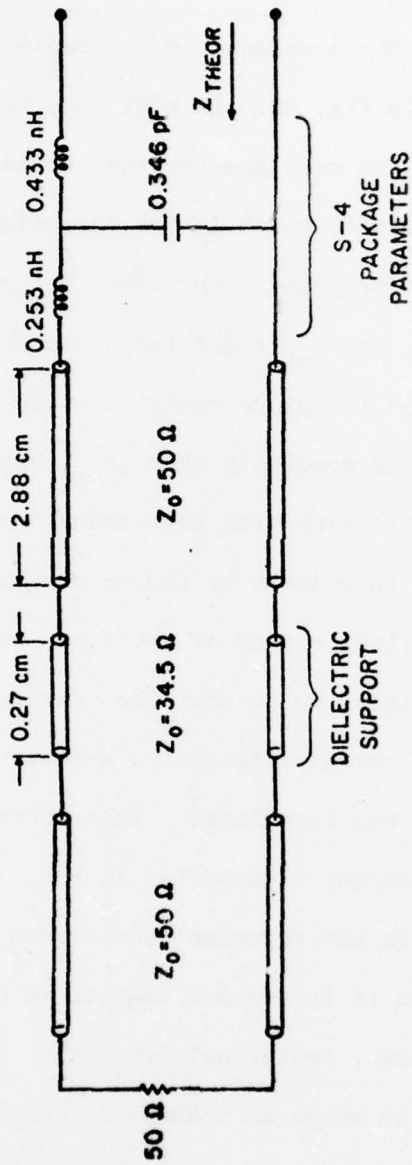


FIG. 23 CIRCUIT USED FOR CALCULATING THE THEORETICALLY EXPECTED IMPEDANCE IN FIG. 21.

analyzer. In general Γ_{mi} will not be exactly equal to Γ_{Ti} , because the network analyzer introduces systematic errors in the measurement system. The error correction procedure consists of obtaining three measurements, the Γ_{mi} 's, corresponding to the three known terminations, the Γ_{Ti} 's. Then Eq. 20 is used to obtain an S-parameter characterization for the measurement errors. If the S-parameters are denoted by S_{oo}^e , S_{o1}^e , and S_{11}^e , then for any future measurement for an unknown termination, Γ_{mu} , a corrected estimate for the actual reflection coefficient of the unknown can be obtained by writing

$$\Gamma_{Tu} = \frac{\Gamma_{mu} - S_{oo}^e}{(S_{o1}^e)^2 + S_{11}^e (\Gamma_{mu} - S_{oo}^e)} \quad (23)$$

Depending on the accuracy to which the Γ_{Ti} standards are known, and the precision with which the Γ_{mi} can be read from the network analyzer, Eq. 23 should be capable of eliminating all linear errors in the measurement system.

The measurement of the empty cavity with the dielectric support was repeated, incorporating the S-parameter algorithm and the error correction procedure; the results are given in Fig. 24. It is seen that as a result of the error correction the measured curves are much smoother than those of Fig. 22. The agreement between measured and theoretical results is reasonable for the imaginary part, although a better circuit model is needed to obtain good agreement.

Figure 25 shows the measured and theoretical impedance (with error correction) for the amplifier circuit, with the seven stepped coaxial sections and the metallized ceramic disk surrounding the package. In this figure, Z_{THEOR} is the impedance of the eight sections

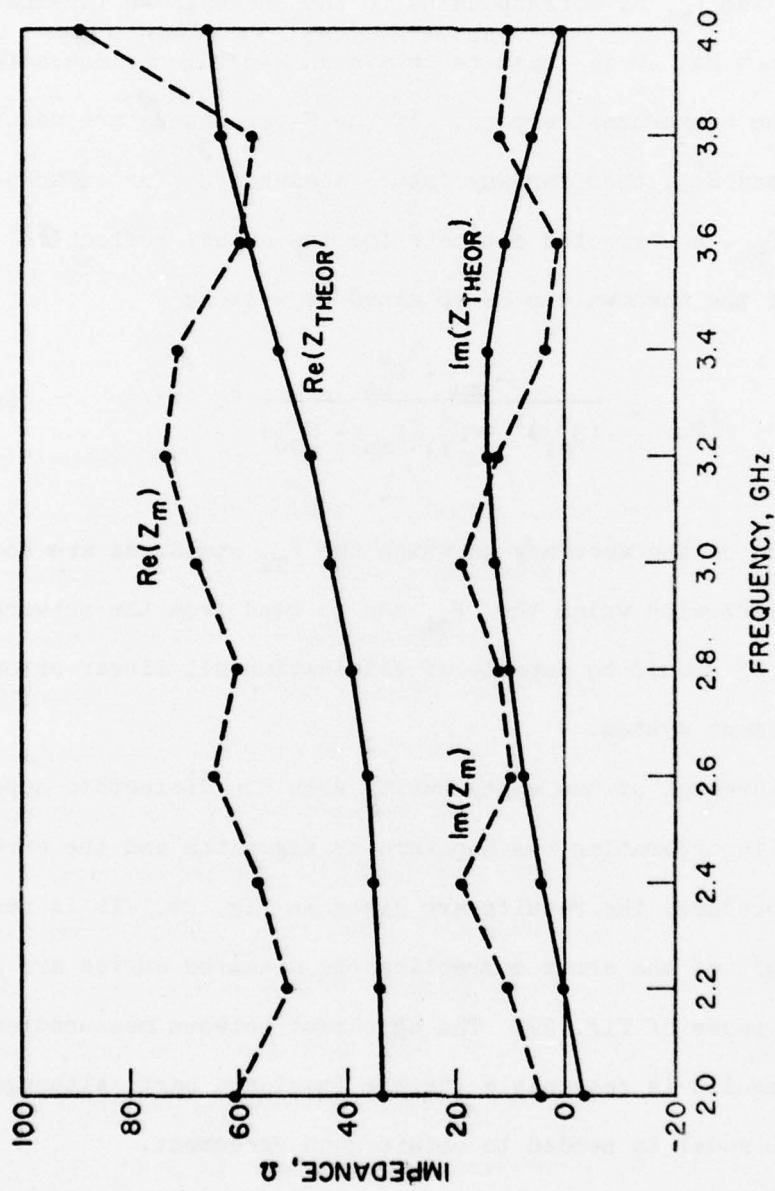


FIG. 24 MEASURED AND THEORETICALLY EXPECTED IMPEDANCE FOR EMPTY COAXIAL LINE WITH ERROR CORRECTION.

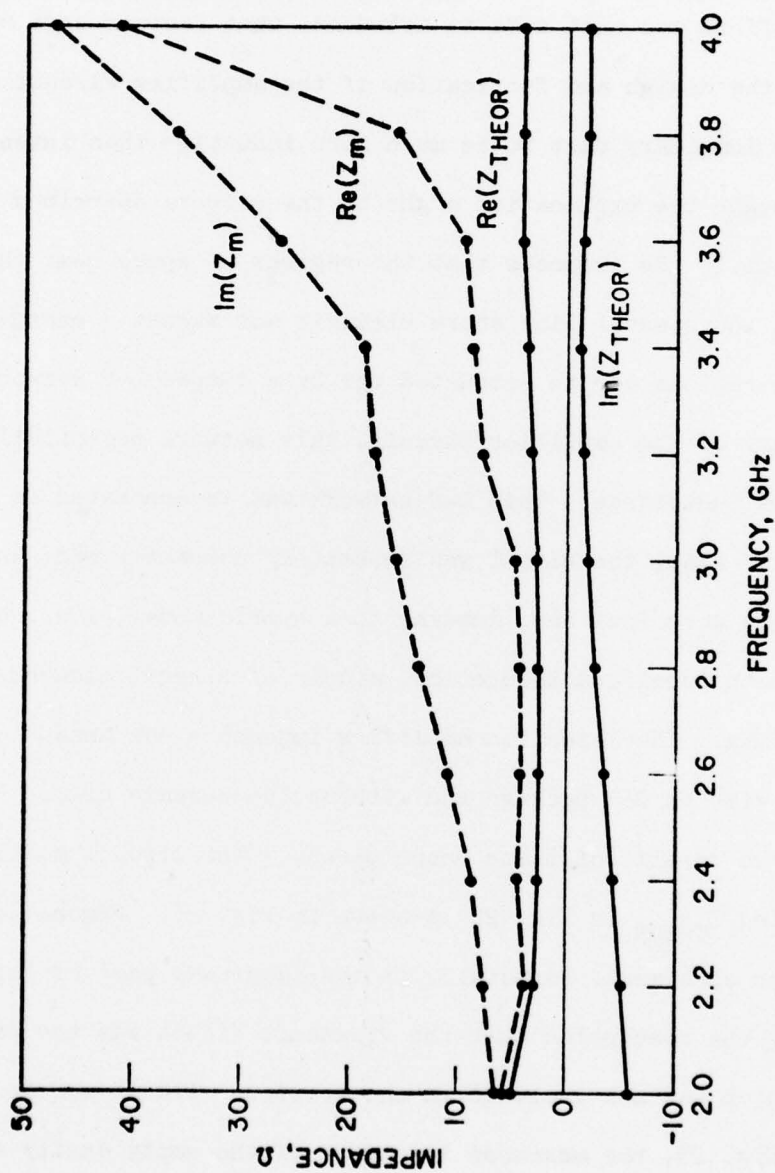


FIG. 25 MEASURED AND THEORETICALLY EXPECTED IMPEDANCE OF THE AMPLIFIER CIRCUIT WITH ERROR CORRECTION.

given in Table 5, terminated in 50Ω . The major element that this model neglects is the bias T. It should be noted that the imaginary part of the impedance is inductive, whereas it was designed to be small and capacitive in this frequency range.

An effort was next made to determine what factors were overlooked in the design and fabrication of the amplifier circuit which caused the imaginary part to be much more inductive than intended. It was thought the explanation might be the effects described recently by Eisenhart.¹² He proposes that the regions of space near the diode package in the coaxial line store electric and magnetic energy and that these regions can be accounted for by a lumped L-C network. For the geometry of the amplifier circuit, this network essentially reduces to a series inductance. This L-C network was incorporated in the circuit model. Also, the bias T was separately characterized, and these measurements were included, leading to a hybrid model, i.e., one which includes both idealized theoretical models of circuit elements and measured data. The 7-section amplifier impedance was measured, in this case with an S-4 package and without the ceramic disk. Figure 26 shows the results of these measurements. The circuit model used in computing Z_{THEOR} in Fig. 26 is shown in Fig. 27. Figure 26 shows much better agreement, especially in the imaginary part of impedance, supporting the conclusion that the Eisenhart effect was the significant element which was not included in the previous circuit models.

In Fig. 28, the measured impedance of the empty cavity already plotted in Fig. 24 is repeated. However, Z_{THEOR} was calculated from a circuit model which, in addition to the elements shown in Fig. 23, includes the Eisenhart mounting parasitics and the measured

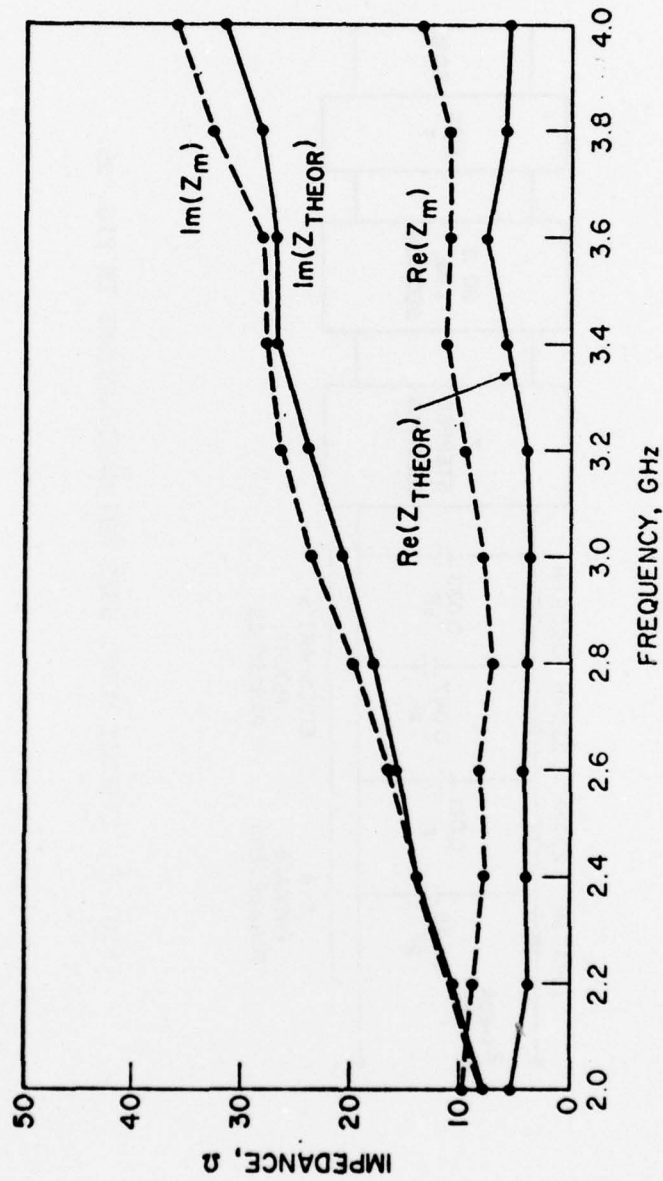


FIG. 26 MEASURED AND THEORETICAL IMPEDANCE OF AMPLIFIER CIRCUIT WITH S-4 DIODE PACKAGE AND WITHOUT CERAMIC DISK.

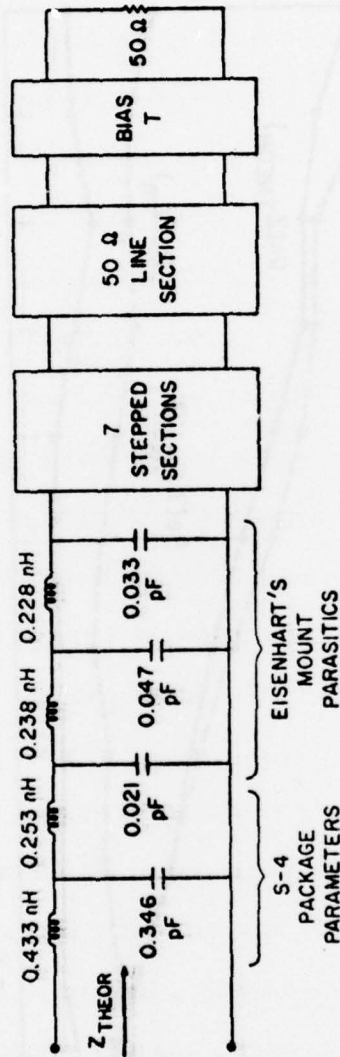


FIG. 27 CIRCUIT MODEL USED FOR CALCULATIONS IN FIG. 26.

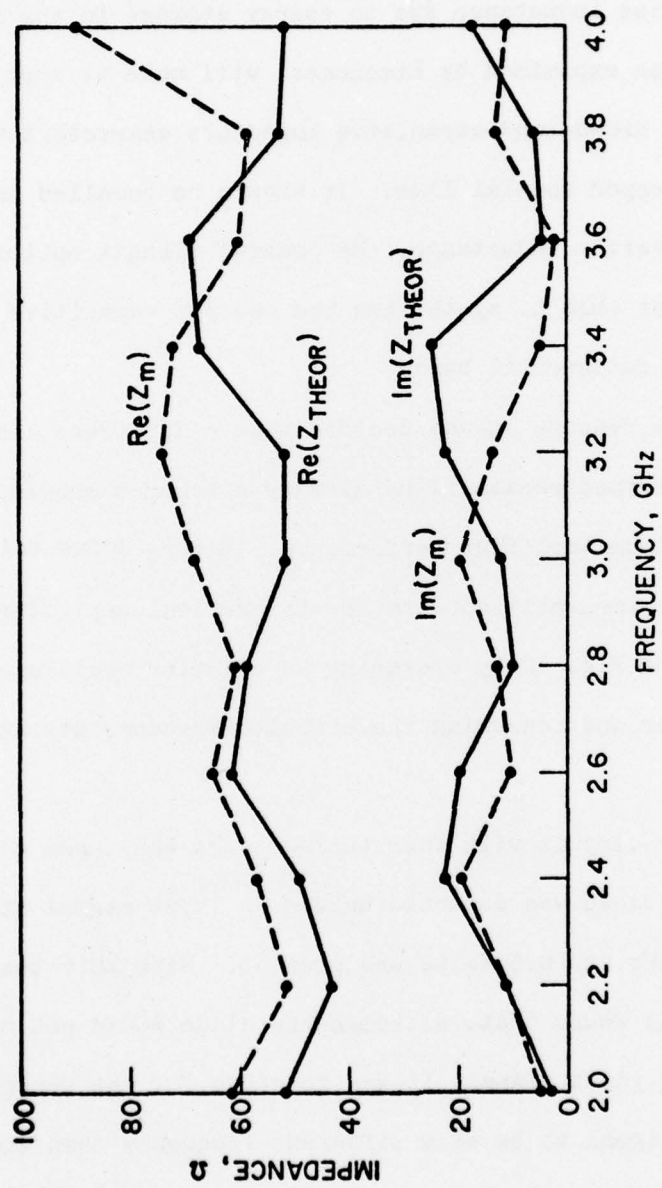


FIG. 28 MEASURED IMPEDANCE OF FIG. 24 WITH THEORETICAL IMPEDANCE OF AN IMPROVED CIRCUIT MODEL.

characterization of the bias T. A substantial improvement in agreement of the resistive parts should be noted by comparing the two figures.

Thus it appears that even with the package lead inductance minimized, the series inductance due to energy storage in the regions near the package, as explained by Eisenhart, will make it very difficult to obtain the broad-band capacitive impedance characteristics of Fig. 12 using a stepped coaxial line. It should be recalled that, even without this series inductance, the coaxial circuit optimization program was not able to synthesize the desired capacitive $\text{Im}\{Z_s\}$ outside the fundamental band.

For the above reasons it was decided that a different kind of circuit from the stepped coaxial line already discussed should be fabricated for optimum amplifier performance. Before doing this, it was decided to experimentally confirm the theoretical amplifier impedance requirements of Fig. 12 by operating an existing oscillator circuit as an amplifier and measuring the circuit impedance at the frequency of amplification.

An oscillator circuit with four tuning slugs was tuned so that no output from the diode was detected unless an input signal at approximately 2.2 GHz and 0.6 Watts was present. With this tuning slug configuration it was found that, although the diode would not operate without an external input signal, it was possible for the generated fundamental diode signal to be at a different frequency than the input signal even with the input signal present. If the frequency of the input was varied from 2 GHz to well above the midband point at 2.2 GHz with the amplifier output monitored on a spectrum analyzer,

the following sequence of events was observed. With the input frequency below the midband frequency by more than approximately 50 MHz, there was no signal generated by the diode except wideband noise well below the input level. As the frequency of the input signal was brought within 50 MHz of the midband frequency, a noticeable diode signal began to appear at the midband point, i.e., at a frequency different from the input frequency. This separate diode signal continued to build up until the input frequency came to within 2 MHz of midband. At this point, the diode signal shifted over and locked with the input signal. The two signals remained locked together for approximately 3 MHz. If the input frequency was further increased, the diode signal returned to its midband frequency value and its amplitude decreased until the input frequency was approximately 50 MHz above midband, at which point only low level noise was detectable from the diode. At any frequency within the 100 MHz range, if the input signal was removed, the diode signal also disappeared. The midband gain observed for this circuit configuration was 8.6 dB.

The circuit is being optimized to improve the amplifier characteristics, and equipment is being set up to measure the impedance vs. frequency characteristics up to the third harmonic, using the de-embedding method. Also, a lumped element TRAPATT oscillator circuit operating in the 800 MHz range is being used as an amplifier, and similar impedance vs. frequency measurements are being made. This data will be compared with the previously obtained theoretical amplifier impedance, and the two sets of impedance data will be used in designing future amplifier circuits.

V. CONCLUSION

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A description has been given of the device simulation computer program which is the basis of the theoretical results obtained. Different methods for obtaining solutions using this program with current drive and voltage drive have been discussed, and a particular current drive yielding negative resistance at least up to the third harmonic has been presented. It was demonstrated that a one cycle simulation is sufficient to characterize the diode impedance, thus avoiding the time and expense of obtaining converged solutions. From a series of diode simulations at different frequencies, the required impedance vs. frequency characteristics for a broadband amplifier was presented. An optimization procedure was discussed whereby the parameters of a stepped coaxial line are adjusted so that the input impedance approximates the required theoretical impedance as closely as possible. The fabrication of the resulting circuit was outlined. Impedance vs. frequency measurements of the fabricated circuit were presented and reasons given for discrepancies between the measured circuit impedances and the expected impedance based on the original circuit model. Finally, experimental results for an amplifier circuit were given as well as suggestions for future measurements and circuit fabrication modifications.

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